Study Material for DSP and its Applications

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Aim:

To generate PWM pulses using TMS 320 F2182 DSP Processor.

Pre MCQ

1. In pulse width modulated inverters, the output voltage is controlled by controlling the
   a) input frequency
   b) modulating index
   c) amplification factor
   d) none of the mentioned

Ans: b

2. In case of sinusoidal pulse width modulation with MI < 1, if the number of pulses per half cycle (N) = 5, then
   a) harmonics of order 5 and 7 become significant
   b) harmonics of order 5 and 7 are eliminated
   c) harmonics of order 9 and 11 become significant
   d) harmonics of order 9 and 11 are eliminated

Ans: c

3. In case of sinusoidal pulse width modulation with MI < 1, the order of the dominate harmonic can be raised by
   a) increasing the number of pulses
   b) reducing the number of pulses
   c) lowering the input voltage frequency
   d) raising the input voltage frequency

Ans: a

4. In case of sinusoidal pulse width modulation with MI < 1, if the number of pulses per half cycle (N) = 6, then

   a) harmonics of order 7 and 9 become significant

   b) harmonics of order 7 and 9 are eliminated

   c) harmonics of order 11 and 13 become significant

   d) harmonics of order 11 and 13 are eliminated

Ans: c

5. Increasing the number of pulses (N), _____

   a) reduces the output voltage amplitude

   b) reduces the inverter efficiency

   c) improves the inverter efficiency

   d) none of the mentioned

Ans: b

PWM Output and General Purpose Timer Compare Operation

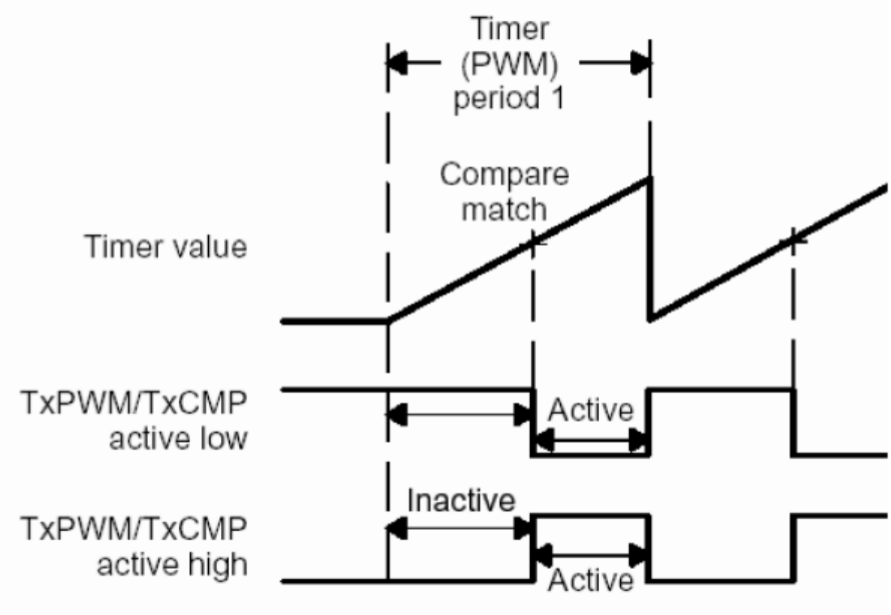
A PWM waveform is a sequence of pulses with fixed frequency but varying pulse widths. The width of the pulse might vary from 0% to 100% of the fixed period. The pulse widths are modulated by another signal called the modulation signal. In order to generate a PWM signal digitally, a timer is set to continuously repeat a counting period. This period is known as the PWM carrier period. The inverse of the carrier period is called the carrier frequency.

The counting pattern of the timer will either be a “saw-tooth” (asymmetric) or “triangle” (symmetric) wave depending on what counting mode the timer has been configured for. As always, the compare value is constantly being compared with the value of the timer counter. When a match occurs, the output toggles High to Low, or Low to High. When the timer period value is reached or a second match occurs, the output toggles again. The on and off time of the pulse is directly dependent on the value loaded into the timer’s compare register. By varying the number in the compare register by the modulation signal (usually a sinusoid), a PWM signal that represents the modulating signal can be produced.

The “output” discussed above refers to each GP Timer’s associated PWM output pin (TxPWM). The logic level of the PWM output pin is determined automatically by hardware.

This level is based on the value of the associated compare register and timer count value (see Fig. 1, note the compare match points and the output change at these points). If the compare operation is enabled in TxCON, the following events occur on a compare match:

1. The compare interrupt flag of the timer is set one clock cycle after the match.
2. A transition occurs on the associated PWM output pin one device clock cycle after the match according to the bit configuration in GPTCONA/B.
3. If the compare interrupt flag has been selected by the appropriate GPTCONA/B bits to start the ADC, an ADC start signal is generated at the same time the compare interrupt flag is set.
4. A peripheral interrupt request is generated by the compare interrupt flag if it is unmasked.



+ Compare matches

Figure 1 Timer compare match and associated change on TxPWM pin.

The polarity of the compare output of a GP Timer can be specified active high, active low, forced high, or forced low. This polarity is determined by setting the bits in the GPTCONA/B register. If active low, the output changes from high to low on the first compare match. It then goes from low to high on the second compare match if the GP Timer

is in an up/down-counting mode, or on period match if the GP Timer is in up-counting mode. If active high, the output changes from low to high on the first compare match. It then goes from high to low on the second compare match if the GP Timer is in an up-/down counting mode, or on period match if the GP Timer is in up-count mode. If forced low, the timer compare output becomes low immediately when it is specified. If forced high, the timer compare output becomes high immediately when it is specified.

By default (after a reset or power-on) all GP Timer PWM output pins are put in a high-impedance (HI-Z) state. The PWM output must be made active by configuring the GPTCONA/B registers. At anytime the PWM outputs will be made HI-Z whenever the power drive protection pin PDPINTx is active and is pulled low. Additionally, the corresponding PWM pin will be made HI-Z when bit 1 of the TxCON register is zeroed by software.

The transition on the PWM output pin is controlled by the asymmetric or symmetric timer waveform and the associated output logic. For an asymmetric wave form, the timer is set up in continuous up-count mode. To generate a symmetric waveform, the timer needs to be configured to continuous up/down counting.

Example 1 - Generation of an Asymmetric Waveform:

The asymmetric waveform in Fig. 2 is generated when the GP Timer is in continuous up-counting mode. When in this mode the output changes in the following:

1. Output pin at “inactive level” before the counting operation starts
2. Output pin remains at “inactive level” until the compare match happens
3. Output toggles to “active level” on the compare match
4. Output remains unchanged at “active level” until the end of the period
5. At end of period, output resets to “inactive level”; that is if the new compare value is not zero

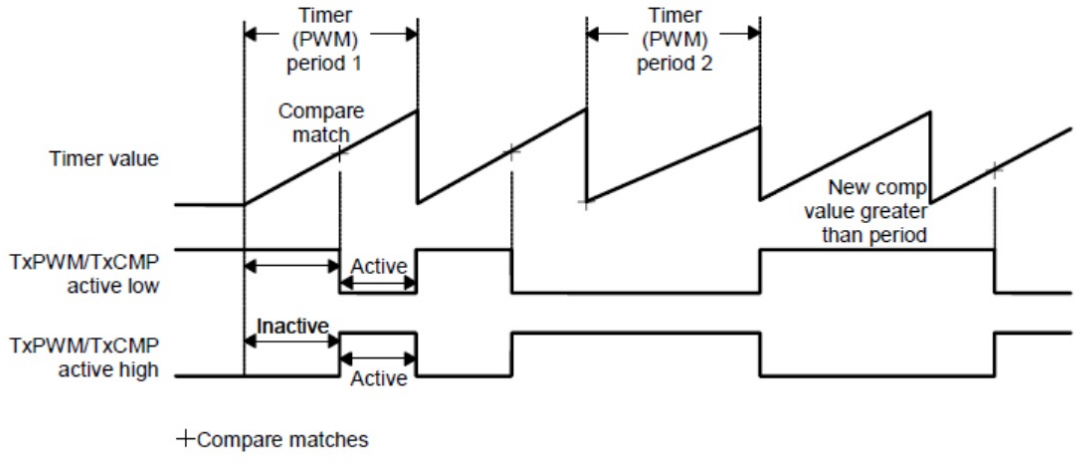


Figure 2 Asymmetric timer waveform generated by a GP timer in continuous up-count mode.

If the compare value is zero at the very beginning of the period, then a compare match is made at the very beginning and, consequently, the output is the active level for the period. If the output is “active” for the whole period and the new compare value for the next period is zero, then the output will stay at the active level so as not to cause a glitch. If the value in the compare register is greater than the value in the period register, then a compare match will never be made and consequently the output will be at the inactive level through the whole period.

The above allows the duty cycle of the PWM to range from 0 to 100% without glitches being present. If the compare value is the same as the period value, which causes a compare match, then the output pin will be at the active level for exactly one pre-scaled clock cycle.

Example 2 - Symmetric Waveform Generation:

When the GP Timer is configured in continuous up/down-counting mode, a symmetric waveform is generated as in Fig. 3. The output changes in the following sequence:

1. “inactive level” before the counting operation starts
2. remains at “inactive level” until the compare match
3. toggles to “active level” on the first compare match
4. remains unchanged at “active level” until the second compare match
5. toggles to “inactive level” on the second compare match
6. remains unchanged at “inactive level” until the end of the period and remains unchanged until next compare match

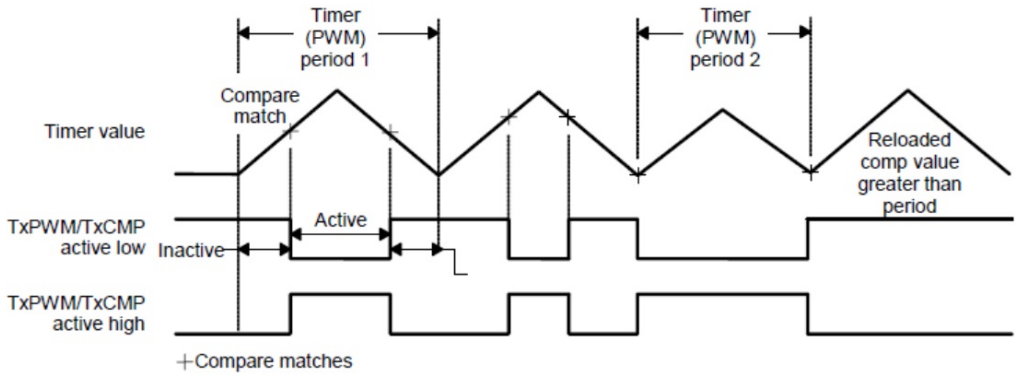


Figure 3 Symmetric timer waveform from continuous up/down count mode.

If the compare value is zero at the beginning of the period, the output is set to the active level at the beginning of a period and remains unchanged until the second compare match. After the first transition, the output remains at the active level until the end of the period if the compare value becomes zero for the second half of the period. When this happens, the output does not reset to zero if the new compare value for the following period is still zero. This is done again to assure the generation of PWM pulses of 0% to 100% duty cycle without any glitches. The first transition does not happen if the compare value is greater than or equal to that of the period register for the first half of the period. However, the output still toggles when a compare match happens in the second half of the period. This error in output transition, often as a result of calculation error in the application routine, is corrected at the end of the period because the output resets to zero, unless the new compare value for the following period is zero. In this case, the output remains one, which again puts the output of the waveform generator in the correct state.

Calculations for Active and Inactive Time Periods

In order to utilize the GP Timer PWM outputs, it is sometimes necessary to calculate the active and inactive pulse times for the PWM output pins. We can find the active and inactive times for both the asymmetrical (Continuous Up-Count Mode) and symmetrical (Continuous Up/Down Count Mode). The calculation criteria for these times are as follows:

Continuous Up-Count Mode:

Active Output Pulse Time = [(TxPR) – (TxCMPR) + 1] cycles of the scaled input clock.

Inactive Output Pulse Time = (period of the scaled input clock) * (value of TxCMPR)

- When the value in TxCMPR is zero, the GP Timer compare output is active for the whole period.
- When TxCMPR is TxPR, the length of the active phase (the output pulse width) is zero.

Continuous Up/Down Counting Mode:

For the continuous up-/down-counting mode, the compare register can have different values while counting down and while counting up.

Active Output Pulse Time = [(TxPR) – (TxCMPR)**up** + (TxPR) – (TxCMPR)**dn**]** cycles of the scaled input clock

- If (TxCMPR) **up** is zero, the compare output is active at the beginning of the period. If (TxCMPR)dn is also zero, then output remains active until the end of the period.
- When (TxCMPR)**up** is (TxPR), the first transition is lost. Similarly, the second transition is lost when (TxCMPR)**dn** is (TxPR).
- If both (TxCMPR)up and TxCMPR)dn are greater than or equal to (TxPR), then the GP Timer compare output is inactive for the entire period.

**where (TxCMPR)up is the compare value on the timer's way up and (TxCMPR)dn is the compare value on the way down.

GP Timer PWM Generation -Practical Steps

To generate a PWM output signal on the GP Timer PWM outputs, make sure the following are configured to allow for PWM generation (also see Example 6.3): 1. Note what the PLL module is set to. The PLL provides the clock signal to the DSP and hence to the EV. In the timer control registers we have the option of pre-scaling (dividing) the clock signal to choose a time base for the GP Timers.

2. The corresponding EV pins need to be configured for their primary function in the appropriate MCRx register.

3. Initialize TxCNT (we usually set the count vale to zero)

4. Set TxPR according to the desired PWM (carrier) period. The TxPR value is calculated by the following formulas:

Asymmetric PWM:

$$\text{TxPR Value} = \left[\frac{\textit{desired PWM period}}{\textit{GP Timer prescaled clk period}} - 1 \right]$$

Symmetric PWM:

$$\text{TxPR Value} = \left[\frac{desired\ PWM\ period}{2 * (GP\ Timer\ prescaled\ clk\ period)} \right]$$

5. Initialize TxCMPR to first desired compare value
6. To create a PWM signal, the registers GPTCONA/B and TxCON need to be configured for TxCMP enabled, desired counting mode etc.
7. To create an asymmetric PWM signal, the timer is set to the Continuous-Up Count Mode. If a symmetric PWM signal is desired, then the Timer should be set to the Continuous-Up/Down Mode.
8. During run time, the GP Timer compare register (TxCMPR) will need to be periodically updated with new compare values corresponding to the modulation signal or new duty cycle. This can be done during an interrupt service routine.

Example 3 - Fixed Duty Cycle PWM

The following block of code is an example of generating a simple fixed-duty cycle PWM signal by using the GP Timer Compare function. The PLL needs to be set to CLKIN x 4, the watchdog needs to be disabled, and the wait state generator (WSGR) set for zero wait states.

```
LDP    #SCSR1>>7
SPLK  #000Ch,SCSR1          ;EVA & EVB modules clock enable
LDP    #0E1h            ;Set Mux pins for
SPLK #0FFFFh,MCRA          ;PWM function
SPLK #0FFFFh,MCRC          ;EVA PWM output initialization
LDP    #GPTCONA >> 7h ;Load EVA data-page
SPLK #00000h, T1CNT ;this just zeros the counter T1 the
                           ;counters are auto zeroed after a DSP
                           ;reset
SPLK #0FFFFh, T1PR         ;the T1PR value sets the frequency in
                           ;this case, it is 500 Hz cont up-cnt mod
SPLK #08000h, T1CMPR;50 % duty cycle PWM bits---
SPLK #0000000001000010b, GPTCONA
SPLK #1001000001000010b, T1CON
LOOP2 B LOOP2              ;after the control registers are setup
                           ;the program can loop endlessly while
                           ;PWM is generated automatically
```

4 Compare Units

A PWM signal can also be generated using the compare unit (CMPRx). The compare units (CMPRx) in the LF2407 function identically to the GP Timer compare units (TxCMPR) discussed above. Unlike the GP Timer compare function, each compare unit has two associated PWM outputs which both toggle on the same compare match. The PWM outputs associated with the compare units allow for the generation of six PWM outputs per EV.

As shown in Fig. 4 the Compare Units Include:

- Three 16-bit compare registers (CMPR1, CMPR2, and CMPR3 for EVA; and CMPR4, CMPR5, and CMPR6 for EVB), all double-buffered
- One 16-bit compare control register (COMCONA for EVA, and COMCONB for EVB)
- One 16-bit action control register (ACTRA for EVA, and ACTRB for EVB), with an associated buffer register
- Six PWM (3-state; Low, High, High Z) output (compare output) pins (PWMy, y = 1, 2, 3, 4, 5, 6 for EVA and PWMz, z = 7, 8, 9, 10, 11, 12 for EVB)

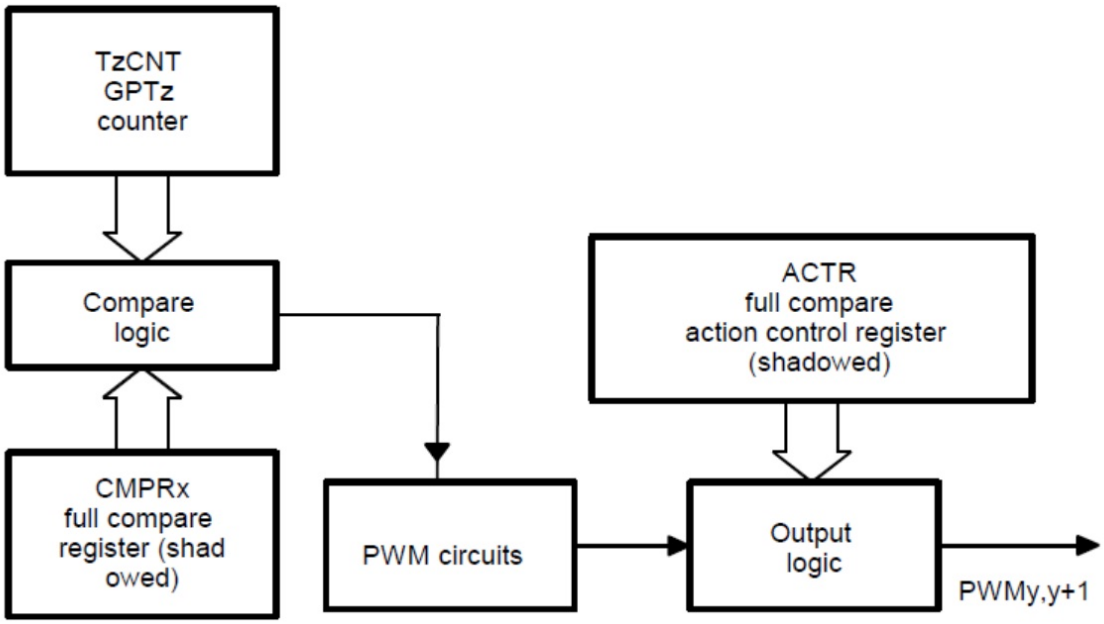


Figure 4 Compare unit block diagram.

For EVA: x = 1, 2, 3; y = 1, 3, 5; z = 1

For EVB: x = 4, 5, 6; y = 7, 9, 11; z = 3

4.1 Inputs and Outputs of the Compare Units

The inputs to a compare unit include:

- Control signals from compare control registers
- GP Timer 1/3 (T1CNT/T3CNT) count value, underflow, and period match signals
- System RESET
- The time base (counter value) for the compare units in EVA (CMPR1,2 ,3) is GP Timer 1, and for EVB (CMPR4, 5, 6) is GP Timer 3.

When any reset event occurs, all register bits associated with the compare units are reset to zero and all compare output pins are put in the high-impedance state. The output of a compare unit is a compare match output, or in other words, a PWM output. If the compare operation is enabled, a compare match signal sets the corresponding interrupt flag and the two output pins associated with the compare unit to toggle. Either of the two outputs can be configured as either active high or active low, but will toggle upon the same event.

4.2 Operation of Compare Units

The sequence below is an example of the compare unit operation in EVA. For EVB operation, GP Timer 3 and ACTRB are used instead:

1. The value of the GP Timer 1 counter is continuously compared with that of the compare register.
2. When a compare match occurs, a transition appears on the two outputs of the compare unit according to the bits in the action control register (ACTRA). The bits in the ACTRA can individually specify each output to toggle active high or toggle active-low (if not forced high or low) on a compare match.
3. The compare interrupt flag associated with a compare unit is set when a compare match is made between GP Timer 1 and the compare register of a compare unit, if compare is enabled.
4. A peripheral interrupt request will then be generated if the interrupt is unmasked. The timing of output transitions, setting of interrupt flags, and the generation of interrupt requests are similar to the GP Timer compare operation.
5. The outputs of the compare units in compare mode are subject to modification by the output logic, dead band units, and the space vector PWM logic.

Having two outputs controlled by the same compare unit is useful in applications such as the control of a power inverter (see Fig. 5). With a power inverter, PWM signals can be used to gate the power transistors for creating currents through the legs of the inverter of any frequency or amplitude. This is useful in controlling electric motors their operation depends on the current flowing through the windings. By controlling the current flowing through motor windings, torque and speed control of the motor can be accomplished.

In inverter circuits such as those shown in Fig. 5, two power transistors are placed in series on each phase "leg" with the output being between them. This allows the output of the leg to be connected either to the DC supply voltage (Vdc) or ground. A potential hazard with these circuits is that if both transistors are turned on at the same time, a short circuit condition will exist through the leg and power transistors, causing the transistors to rapidly heat up and, in most cases, explode.

The solution to this problem is to make sure that only one transistor in each leg is on at a time. In theory, this is accomplished by feeding complementary PWM gating signals to each of the two transistors in a leg. So when one transistor is on, the other is off. In reality, all transistors turn on faster than they turn off. Therefore, it is necessary to add a time delay (dead-band) between the PWM signals to allow for the first transistor to fully turn off before the second one is turned on.

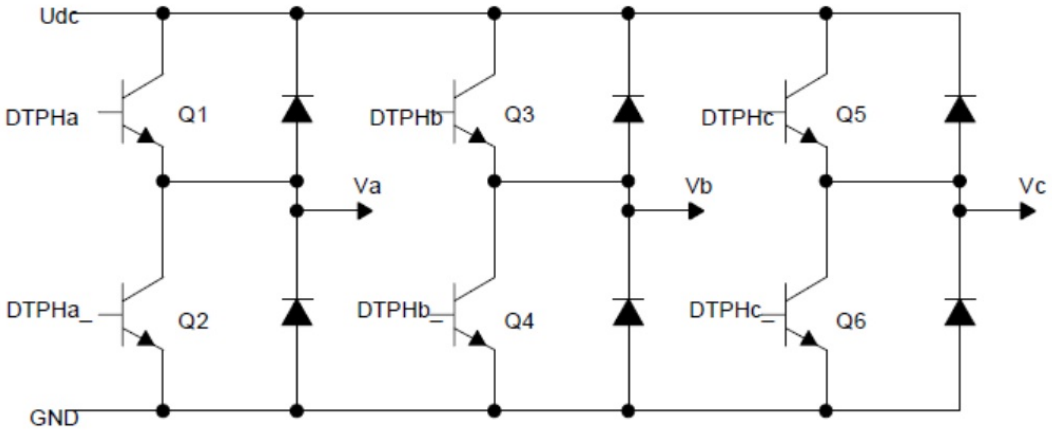


Figure 5 Basic three-phase inverter circuit.

1. Which among the below stated components should be filtered for determining the cut-off frequency corresponding to the PW period of low-pass filter ?
   a. Fundamental F_{PWM} & higher harmonics
   b. Resonant F_{PWM} & higher harmonics
   c. Slowly Varying DC components
   d. Slowly Varying AC components
   Ans: a

2. Three methods for modulating a digital signal with analog data are
   a) PAM, ASM, PPM
   b) PAM, PWM, PPM
   c) FSK, QAM, PAM
   d) QAM, PAM, PWM,

   Ans: b

3. Pulse amplititude modulation makes use of
   a) a successive approximator
   b) a dual-slope ADC
   c) an R/2R set up
   d) a sample and hold circuit

   Ans: d

4. A certain number of bits (D) are encoded by a single pulse in one of 2D possible positions during a specified fixed period (T) in

   a) TDM
   b) PAM
   c) PPM
   d) PWM

   Ans: c