



श्रीचन्द्रशेखरेन्द्रसरस्वतीविश्वमहाविद्यालयः  
(विश्वविद्यालयानुदानयोगस्य १९५६ विधे: तृतीयविधिमनुसृत्य मानितविश्वविद्यालयत्वेन प्रकटीकृतः)

**SRI CHANDRASEKHARENDRASARASWATHI VISWA MAHAVIDYALAYA  
(SCSVMV)**

(Deemed to be University u/s 3 of the UGC Act 1956)  
(Accredited with 'A' Grade by NAAC)  
Enathur, Kanchipuram - 631 561.



25/05/2020

## **Digital Logic Design Using VLSI Webinar Report**

Department of Electrical and Electronics Engineering, SCSVMV University, Enathur, Kanchipuram organised one day webinar on “*Digital Logic Design Using VLSI*” on 22 May 2020, Friday @ 10.00am to 11.00am.

**Speaker** – Mrs. N.Poongodi,  
Professor & Head,  
ECE Department,  
V.Ramakrishna Polytechnic,  
Chennai -19

**About Webinar** – Speaker covers basics of Boolean logic, digital & VLSI design in detail with duration of 2 hours. For all active participants certificates were issued after receiving feedback

**Participants** – Registered – 258 & Active Participants - 95

**Organizers** – 1. **Dr.M.RathinaKumar**

Professor & Head – EEE Dept.

2. **Dr.D.Vanitha,**

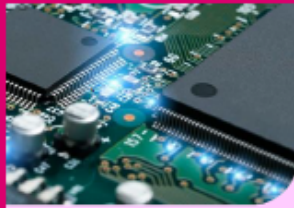
Assistant Professor – EEE Dept.



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**Sri Chandrasekharendra Saraswathi Viswa  
Mahavidyalaya**

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Enathur, Kanchipuram - 631 561, Tamilnadu, India.  
www.kanchiuniv.ac.in



**Department of Electrical and Electronics  
Engineering**

*Organizing*

**WEBINAR**

**DIGITAL LOGIC DESIGN USING VLSI**

On 22<sup>nd</sup> May 2020, Friday @ 10 am - 11 am



**Resource Person**

Mrs. N. Poongodi,  
Professor & Head,  
Department of ECE,  
Ramakrishna Polytechnic,  
Chennai.

**Convener**

Dr. M. Rathinakumar,  
Professor & Head,  
Department of EEE,  
SCSVMV.

**For FREE Registration:**

<https://forms.gle/GSZXfgVg4igcgF1R8>

'E-Certificate' will be provided to all the  
active participants.

**Scan to Register**



**Co-ordinator**

Dr. D. Varitha,  
Assistant Professor,  
Department of EEE, SCSVMV  
Mob.: 9444164917