



CURRICULUM (2023-24) M.E (EMBEDDED SYSTEM TECHNOLOGIES)

CURRICULUM I TO IV SEMESTERS (FULL TIME)

SEMESTER I

S.No:	COURSE CODE	COURSE TITLE	L	Т	Р	С
1.		ADVANCED	4	2	0	4
		MATHEMATICS FOR				
		ELECTRONICS ENGINEERS				
2.		ADVANCED DIGITAL	4	2	0	4
		SYSTEM DESIGN				
3.		MICROCONTROLLER	4	2	0	4
		BASED SYSTEM DESIGN &				
		ANALYSIS				
4.		DESIGN OF EMBEDDED	4	2	0	4
		SYSTEMS				
5.		EMBEDDED	4	2	0	4
		PROGRAMMING				
6.		ELECTIVE I	4	2	0	4
		ΓΟΤΑL	24	12	0	24

SEMESTER II

S.No:	COURSE CODE	COURSE TITLE	L	Т	Р	С
1.		REAL TIME OPERATING SYSTEM	4	2	0	4
2.		SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS	4	2	0	4
3.		EMBEDDED NETWORKING	4	2	0	4
4.		EMBEDDED COMMUNICATION AND SOFTWARE DESIGN	4	2	0	4
5.		ELECTIVE –II	4	2	0	4
6.		ELECTIVE – III	4	2	0	4
7.		EMBEDDED SYSTEM LABORATORY	0	0	3	2
	,	ГОТАL	24	12	3	26



CURRICULUM (2023-24) M.E (EMBEDDED SYSTEM TECHNOLOGIES)

SEMESTER III

S.No:	COURSE CODE	COURSE TITLE	L	Т	Р	С
1.		ELECTIVE – IV	4	2	0	4
2.		ELECTIVE – V	4	2	0	4
3.		ELECTIVE – VI	4	2	0	4
4.		PROJECT WORK PHASE-I	0	0	12	6
	r	ΓΟΤΑL	12	6	12	18

SEMESTER IV

S.No:	COURSE CODE	COURSE TITLE	L	Т	Р	С
1.		PROJECT WORK PHASE-II	0	0	24	12
	r	ΓΟΤΑL	0	0	24	12

Total Credit to be earned for the award of degree is: 24+26+18+12=80

LIST OF ELECTIVES:

ELECTIVE 1:

S.No:	COURSE CODE	COURSE TITLE	L	Т	Р	С
1		ADVANCED DIGITAL SIGNAL PROCESSING	4	2	0	4
2		RISC PROCESSOR ARCHITECTURE AND PROGRAMMING	4	2	0	4
3		WIRELESS AND MOBILE COMMUNICATION	4	2	0	4
4		BIG DATA ANALYTICS	4	2	0	4



CURRICULUM (2023-24) M.E (EMBEDDED SYSTEM TECHNOLOGIES)

ELECTIVE II & III:

S.No:	COURSE CODE	COURSE TITLE	L	Т	Р	С
1		ASIC DESIGN	4	2	0	4
2		ADVANCED EMBEDDED SYSTEMS	4	2	0	4
3		EMBEDDED LINUX	4	2	0	4
4		VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	4	2	0	4
5		PROGRAMMING WITH VHDL	4	2	0	4
6		PRINCIPLE OF ROBOTICS	4	2	0	4
7		APPLICATION OF MEMS TECHNOLOGY	4	2	0	4
8		DIGITAL IMAGE PROCESSING	4	2	0	4

ELECTIVE IV, V & VI:

S.No:	COURSE CODE	COURSE TITLE	L	Т	Р	С
1		EMBEDDED ANALOG INTERFACING	4	2	0	4
2		EMBEDDED AUTOMOTIVE NETWORKING WITH CAN	4	2	0	4
3		EMBEDDED SYSTEM DESIGN USING ARM PROCESSOR	4	2	0	4
4		DISTRIBUTED EMBEDDED COMPUTING	4	2	0	4
5		SMART METERS AND SMART GRID COMMUNICATION	4	2	0	4
6		SOFT COMPUTING TECHNIQUES	4	2	0	4



Course		L	Т	Р	С	IA	EA	ТМ
Code Course Name	ADVANCED MATHEMATICS FOR ELECTRONIC ENGINEERS	3	1	0	3	40	60	100
	FOR ELECTRONIC ENGINEERS					-10		
Course Category			S	yllabus I	Revision		V.	1.0
Pre-		•					•	
requisite								
Course Objec The course sho	ould enable the students -							
	1. To encourage students to develop a we	orkir	ng kr	nowledge	e of the ce	entral	ideas	of
	linear algebra.		U	U				
	2. To study and understand the concepts	of p	robal	bility and	d random	varia	ble of	the
	various functions.							
	3. To understand the notion of a Markov	chai	in, ar	nd how s	imple ide	as of		
	conditional probability and matrices ca			•	e a thorou	igh an	d	
	effective account of discrete-time Mar	kov	chai	ns.				
	4. To formulate and construct a mathema	itica	l mo	del for a	linear pro	ogran	nming	
	problem in real life situation.							
	5. Introduce the Fourier Transform as an					iques	on	
	periodic functions and to solve partial			-				
	6. To develop the use of matrix algebra t	echn	ique	s this is i	needed by	y eng	ineers	for
	practical applications.							
Course Outco	mes:							
	n of the course, the student will be able to							
Course	Desc	ripti	on					
Outcomes								
CO1	Develop knowledge and understanding in	the	field	ls of line	ar algebra	a.		
CO2	Develop knowledge and understanding in	n the	field	ls of prol	bability.			
CO3	Develop knowledge and understanding ir	n the	field	ls stocha	stic proce	ess.		
CO4	Develop knowledge and understanding ir	n the	field	ls of line	ar matrix			
CO5	Develop knowledge and understanding ir	the	field	ls of Fou	rier trans	form.		
	1							



	LINEAR ALGEBRA	12Hours
Vector spa	aces – norms – Inner Products – Eigen values using QR trans formations –	QR
factorizati	on - generalized eigenvectors - Canonical forms - singular value decompo	osition and
application	ns – pseudo inverse – least square approximations -Toeplitz matrices and s	some
application	ns.	
UNIT-II	ONE DIMENSIONAL RANDOM VARIABLES	12 Hours
properties	variables - Probability function – moments – moment generating func – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma ons –Function of a Random Variable.	
UNIT-III	MATRIX THEORY	12 Hours
-	portant matrix factorizations – The Cholesky decomposition – Q R factor ethod – Singular value decomposition - Toeplitz matrices and some applic	
U NIT-IV	QUEUEING MODELS	12 Hours
	rocess – Markovian queues – Single and Multi-server Mode ls – Little's fo	
	ce Model – Steady State analysis – Se If Service queue.	
JNIT-V	FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS	12 Hours
functions	ransforms: Definitions, properties-Transform of elementary functions – Convolution theorem – Parseval's identity – Solutions to partial different tions, Wave equations, Laplace and Poison's equations.	
	Total Hours	60 Hours
Text Bool		
1.	Bronson, R.Matrix Operation, Schaum's outline series, Mc Graw Hill, (1989).	New york
2.	Oliver C. Ibe, "Fundamentals of Applied Probability and Random Proc Academic Press, (An imprint of Elsevier), 2010.	esses,
3.	Taha H.A. "Operations Research : An introduction" Ninth Edit ion, Pea Asia, New Delhi 2012. ACC.NO: B120195	arson Education,
4.	Sankara Rao, K. "Introduction to partial differential equations" Prentice pvt, Ltd, New Delhi, 1997. ACC.NO: B58352	e Hall of India,
5.	Andrews, L.C. and Philips. R.L. "Mathematical Techniques for engineer scientists", Printice Hall of India, 2006.	ring and
6.	O'Neil P.V. "Advanced Engineering Mathematics", (Thomson Asi a pr Singapore) 2007, cengage learning India private limited ACC.NO: B1	
	Singapore) 2007, cengage learning india private initied ACC.NO. BI	17033



Course Code		L	Τ	Р	С	IA	EA	TM
Course Name	ADVANCED DIGITAL					10	6.0	100
	SYSTEM DESIGN	3	1	0	3	40	60	100
Course			Sylla	bus R	levisi	on	V	7.1.0
Category			U					
Pre-requisite								
Course Objectiv	/es:							
The course shoul	d enable the students -							
	1. Basics on Synchronous & As	ynchro	nous o	ligital	swit	ching d	lesign.	
	2. Design & realisation of error	free fu	nction	al blo	cks f	or digit	al system	ns
Course Outcom	es:							
On completion of	f the course, the student will be able to)						
Course		Descri	ption					
Outcomes								
CO1	Develop knowledge and unders		g in	the	basic	s on	Synchr	onous &
	Asynchronous digital switching des		1	1 .			1. D'	· 1
CO2	Develop knowledge and understan	nding	in the	basi	cs of	n Fau	lit Diagi	nosis and
CO3	Testability Algorithms Develop knowledge and understand	ingin	haha		n Cu	nahran	oug Dog	ion Using
COS	Programmable Devices.	ing in	ine da	sics of	n Sy	nemon	ous Des	ign Using
CO4	Develop knowledge and unders	tanding	r in	the	hasic	s on	Synchr	onous &
0.04	Asynchronous digital switching							
	functional blocks for digital system							
	language.		<i>J</i>	<u>-</u>		0		I.
CO5	Develop knowledge and unders	tanding	g in	the	basic	s on	Synchr	onous &
	Asynchronous digital switching							
	functional blocks for digital system	s and s	ystem	ı desig	gn us	ing har	dware d	escriptive
	language.							
					~~~~~			
UNIT-I	SEQUENTIAL & ASYNCHRON						12 Ho	
2	ked Synchronous Sequential Networl	`			•			
-	Reduction – Design of CSSN – Desi	-						
Realization, De	sign of Arithmetic circuits for F	Fast ac	lder-	Array	y M	ultiplie	r. Anal	ysis of
Asynchronous S	Sequential Circuit (ASC) - Flow T	able F	Reduct	tion -	- Ra	ce s in	n ASC	– State
Assignment – Pr	oblem and the Transition Table - De	sign of	ASC	– Sta	tic a	nd Dyn	amic Ha	azards –
Essential Hazard	ds – Data Synchronizers – Design	ing V	endin	g Ma	chine	e Cont	roller –	Mixed
Operating Mode	Asynchronous Circuits.							
UNIT-II	FAULT DIAGNOSIS AND TEST	ABIL		LGO	RIT	HMS	12 Ho	urs
Fault Table Meth	nod – Path Sensitization Method – Bo	olean I	Differe	ence N	/lethc	od – Ko		
	chniques – The Compact Algorithm							•
	sking Cycle – DFT Schemes – Built-i				~			
Seneration Mu	Same Spere Dri Senemes Dunti							



# UNIT-III SYNCHRONOUS DESIGN USING PROGRAMMABLE 12 Hours DEVICES 12 Hours

Programming Techniques -Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array Logic; Architecture and application of Field Programmable Logic Sequence.

UNIT-IV	NEW GENERATION PROGRAMMABLE LOGIC	12 Hours
	DEVICES	

Fold back Architecture with GAL, EPLD, EPLA, PEEL, PML; PROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000.

UNIT-V SYSTEM DESIGN USING VHDL

12 Hours

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modelling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits – VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

	Total Hours 60 Hours
Text Book(s)	
1.	Donald G. Givone, "Digital principles and Design", Tata McGraw Hill 2002. ACC.NO: B100970
2.	Mark Zwolinski, "Digital System Design with VHDL", Pear son Education, 2004.
3.	Stephen Brown and Zvonk Vranesic, "Fundamentals of Digital Logic with VHDL Deisgn", Tata McGraw Hill, 2002
4.	John M Yarbrough, "Digital Logic applications and Design", Thom son Learning, 2001
5.	Parag K Lala, "Digital System design using PLD", BS Publications, 2003
6.	Nripendra N Biswas, "Logic Design Theory", Prentice Hal 1 of India, 2001 ACC.NO: B130827
7.	Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004. ACC.NO: B134442
8.	Navabi.Z. "VHDL Analysis and Modelling of Digital Systems, McGraw International, 1998.



Course Code		L	Т	Р	С	IA	EA	ТМ
Course Name	MICROCONTROLLER							
	BASED SYSTEM DESIGN	3	1	0	3	40	60	100
Course			Sylla	bus R	evisi	on		V.1.0
Category			-					
Pre-requisite								
Course Objectiv								
The course shou	ld enable the students -							
	Basic understanding of embedded sys			-			•	-
	specifications, architectural and detaile	ed de	esign,	and i	mple	mentat	ion, foc	using on real-
	time applications. Learning the conce	pts v	vill be	e enfo	orced	by a	Project	to design and
	develop an embedded system based on	a sin	gle-ch	ip mi	croco	ontrolle	r.	
<b>Course Outcom</b>	es:							
On completion of	f the course, the student will be able to							
Course		Dese	criptio	on				
Outcomes								
<b>CO1</b>	Develop knowledge and understand							
	architectural and detailed design, and	ımpl	ement	ation,	focu	ising or	n real-tii	me application
CO2	of 8051. Develop knowledge and understand	lina	on th		atom	raquir	omonto	anaifiantian
02	architectural and detailed design, and							
	of 32 bit ARM 920	mpi	cincin	ation,	1000	ising of	i icai-tii	
CO3	Understanding on the system requir	reme	nts sp	oecific	atior	ns, arcl	nitectura	al and detaile
	design, and implementation of ARM F		-					
CO4	Understanding on the system require	romo	nta ar	- anifi	otior	na aral	aitaature	and dataila
004	design, and implementation of Microc		1			,		
		onnic		ubeu .			-	
CO5		1 hu	Droi	pot to	danie	mond	dovolon	
CO5	Learning the concepts will be enforced			ect to	desig	gn and o	develop	
CO5				ect to	desig	gn and o	develop	
	Learning the concepts will be enforced system based on a single-chip microco			ect to	desig	gn and o	-	an embedded
CO5 UNIT-I	Learning the concepts will be enforced			ect to	desig	gn and o	12 Ho	an embedded
UNIT-I	Learning the concepts will be enforced system based on a single-chip microco	ontrol	ller.				12 Ho	an embedded
UNIT-I Introduction to	Learning the concepts will be enforced system based on a single-chip microco <b>REVIEW OF 8051</b>	- Cl	PU BI	lock (	liagr	am, M	12 Ho emory	an embedded urs Organization,
UNIT-I Introduction to Program memor	Learning the concepts will be enforced system based on a single-chip microco <b>REVIEW OF 8051</b> Embedded System. Architecture, 8051         y, Data Memory, Interrupts Peripheral	- Cl ls: T	PU Bl	lock (	liagr al Po	am, M ort, I/O	<b>12 Ho</b> emory Port F	an embedded urs Organization, Programming:
UNIT-I Introduction to Program memor Addressing Mod	Learning the concepts will be enforced system based on a single-chip microcol <b>REVIEW OF 8051</b> Embedded System. Architecture, 8051         ry, Data Memory, Interrupts Peripheral         les, Instruction Set, Programming Time	- Cl ls: T	PU Bl	lock (	liagr al Po	am, M ort, I/O	<b>12 Ho</b> emory Port F	an embedded urs Organization, Programming:
UNIT-I Introduction to Program memor	Learning the concepts will be enforced system based on a single-chip microcol <b>REVIEW OF 8051</b> Embedded System. Architecture, 8051         ry, Data Memory, Interrupts Peripheral         les, Instruction Set, Programming Time	- Cl ls: T	PU Bl	lock (	liagr al Po	am, M ort, I/O	<b>12 Ho</b> emory Port F	an embedded urs Organization, Programming:
UNIT-I Introduction to Program memor Addressing Mod	Learning the concepts will be enforced system based on a single-chip microcol <b>REVIEW OF 8051</b> Embedded System. Architecture, 8051         ry, Data Memory, Interrupts Peripheral         les, Instruction Set, Programming Time	- Cl ls: T	PU Bl imers,	lock (	liagr al Po	am, M ort, I/O	<b>12 Ho</b> emory Port F	an embedded urs Organization, Programming: ence to 8-bit

32- Bit ARM920T Processor Core -Introduction: RISC/ARM Design Philosophy, About the ARM920T Core, Processor Functional Block Diagram. Programmers Model. Cache: Memory hierarchy and cache memory-. Memory Management Units: - ARM Instruction Set- Thumb Instruction Set. Interrupt Handling.



UNIT-III	ARM PROCESSOR ORGANIZATION	12 Hours					
ARM9 Micr	ocontroller Architecture-Block Diagram, Features, Memory M	apping Memory Controller (MC)-					
External Bus Interface (EBI)-External Memory Interface-Interrupt Controller-System Timer (ST- Real Time							
Clock (RTC	) Parallel Input/output Controller (PIO).						
UNIT-IV	PERIPHERALS OF ARM PROCESSOR	12 Hours					
AT91RM92	00 PERIPHERALS -Universal Synchronous Asynchronous	Receiver Transceiver (USART)-					
Block Diagr	am, Functional Description, Synchronous and Asynchronous M	1odes.					
UNIT-V	<b>DEVELOPMENT &amp; DEBUGGING TOOLS FOR</b>	12 Hours					
	MICROCONTROLLER BASED EMBEDDED SYSTEM	IS					
Software an	d Hardware tools like Cross Assembler, Compiler, Debugge	er, Simulator, In-Circuit Emulator					
(ICE), Logic							
( <i>)//</i> U	, ,						
	Total Ho	ours 60 Hours					
Text Book(s							
1.	Intel Hand Book on "Embedded Microcontrollers", 1 st Editio	n.					
2.	Muhammad Ali Mazidi, Janice Gillispie Mazidi, Ro						
	Microcontroller and Embedded Systems using Assembly and	•					
3.	ARM Company Ltd. "ARM Architecture Reference Manual-	- ARM D DI 0100E".					
4.	4. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; Morga						
	Kaufmann Publishers.						
5.	Andrew N Sloss, Dominic Symes, Chris Wright, "ARI						
	Designing and Optimizing System Software", 2006, Elsevier	•					
6.	Ayala, Kenneth J "8051 Microcontroller - Architecture, I	Programming & Applications", 1 st					
7.	Edition, Penram International Publishing. Steve Furber, "ARM System-on-Chip Architecture", 2	nd Edition Degreen Education					
7.	ACC.NO: B129645.	2 Edition, Featson Education					
8.	Predko, Myke, "Programming and Customizing the 80	051 Microcontroller". 1 st Edition.					
	McGraw Hill International ACC.NO: B100892.						
9.	Schultz, Thomas W, "C and the 8051 Programming for M	fultitask ing", 1 st Edition, Prentice					
	Hall.						
10.	Stewart, James W, Miao, Kai X, "8051 Microcontroller: H	ardware, Software and Interfacing",					
11	2 nd Edition, Prentice Hall.	advation to Draggage Tools and					
11.	Arnold. S. Berger, "Embedded Systems Design - An intr Techniques", Easwer Press.	roduction t o Processes, Tools and					
12.	Raj Kamal, "Microcontroller - Architecture Programming I	nterfacing and System Design" 1 st					
14.	Edition, Pearson Education.						
13.	P.S Manoharan, P.S. Kannan, "Microcontroller based Sys	stem Design", 1 st Edition, Scitech					
	Publications ACC.NO: B113621.						
14.	David Calcutt, Fred Cowan, Hassan Parchizadeh, "8051 M	Micro controllers – An Application					
	based Introduction", Elsevier.						
15.	Ajay Deshmukh, "Microcontroller - Theory & Applications"	", Tata McGraw Hill.					



Course Code		L	Τ	P	С	IA	EA	TM
Course Name	e Name DESIGN OF EMBEDDED 3 1 0							100
Course		Syllabus Revision V.1.0						7.1.0
Category		<b>v</b>						
Pre-requisite								
Course Objectiv								
	ld enable the students -							
	asics Embedded Design Cycle							
2. D	esign & realization of system with tes	ting pro	ocess.					
Course Outcom								
	f the course, the student will be able t							
Course		Descri	ption					
Outcomes CO1	Davalan knowladge and understor	dina ar	tha	bacic	l of a	mhadd	ad grate	ma dazia
COI	Develop knowledge and understan life cycle.	ung or	i ule	Dasies	5 01 6	mbead	eu syste	ms desig
CO2	Develop knowledge and understand	ling on	the ha	sics	fnar	titionin	o decisio	n
CO3	Develop knowledge and understand							
<u>CO4</u>	· ·	-				-		
<u>CO5</u>	<ul><li>Develop knowledge and understanding on the basics of in circuit emulators.</li><li>Develop knowledge and understanding on the basics embedded systems design and an anti-anti-anti-anti-anti-anti-anti-anti-</li></ul>							
	the Testing procedure to be done for the embedded applications.							0
							•	
UNIT-I	EMBEDDED DESIGN LIFE CY	CLE					12 Ho	urs
Embedded Des	sign life cycle - Product specification	– Hard	ware	/ Soft	ware	partiti	oning – 1	Detailed
hardware and	software design - Integration -	Produ	ict te	sting	- 5	Selectio	on Proc	esses –
Microprocessor	r Vs Micro Controller – Performar	nce too	ls –	Benc	h ma	rking	– RTOS	5 Micro
Controller – Pe	erformance tools - Bench marking -	RTOS	availa	ability	/ – T	ool cha	in avail	ability –
	selection processes.			5				5
	r							
UNIT-II	PARTITIONING DECISION 12 Hours							
	cision – Hardware / Software duality -	- co din	σ Har	dwar	- A	SIC rev		
-	Risk – Co-verification – execution		-					
System startup	- Hardware manipulation - memory -	- mappe		055 -	speed			ity.
UNIT-III	INTERRUPT SERVICE ROUTI	NES					12 Ho	urs
Interrupt Servi	ice routines – Watch dog timers –		mem	orv I	Basic	toolse	t – Hos	st based
1	Remote debugging – ROM emulato			2				
	Statistical profiling.	, , , , , , , , , , , , , , , , , , ,	-21 <b>C</b>	mary	201	Cuci		uputor
opunnsation –	Statistical profiling.							



UNIT-IV	IN CIRCUIT EMULATORS	12 Hours				
In circuit emulators - Buller proof run control - Real time trace - Hardware break points -						
Overlay memory	y – Timing constraints – Usage issues – Triggers.					
UNIT-V	TESTING	12 Hours				
Testing – Bug	tracking - reduction of risks & costs - Performance - Unit testin	g – Regression				
testing - Choos	ing test cases - Functional tests - Coverage tests - Testing embed	ded software –				
Performance tes	ting – Maintenance.					
	Total Hours	60 Hours				
Text Book(s)						
1.	1. Arnold S. Berger – Embedded System Design CMP books, USA 2002.					
2.						
3.						



<b>Course Code</b>		L	Т	Р	С	IA	EA	ТМ
Course Name	EMBEDDED PROGRAMMING	3	1	0	3	40	60	100
Course		Syllabus Revision V.						.1.0
Category								
Pre-requisite								
<b>Course Objectiv</b>								
	d enable the students -	1 5						
	o impart the knowledge of the Embedded		U	U				
2.76	o Impart the knowledge in the Application	on w	ith Da	ita Stri	uctur	es.		
<u> </u>								
Course Outcom								
Course	f the course, the student will be able to	comin	otion					
Outcomes	De	scrip	puon					
CO1	Develop knowledge and understandin	σon	the v	arious	nroo	rammi	ng conce	ents user
cor	in the field of embedded.	5 011	the vi	unous	prog	,1 41111111		
CO2	Develop knowledge and understandin	g on	the va	arious	prog	rammi	ng conce	epts used
	in the field of embedded OS fundament	-			1 0	, ,	C	1
CO3	Develop knowledge and understandin	g on	the va	arious	prog	rammi	ng conce	epts use
	in the field of embedded C programming.							
CO4	Develop knowledge and understanding on the various programming concepts used							
	in the field of embedded applications using data structures.							
CO5	Develop knowledge and understanding on the various programming concepts use							epts used
	in the field of embedded java.							
UNIT-I	INTRODUCTION						12 Ho	urs
	ssues in Real Time Computing – Struct	ire o	faRe	eal Tir	ne Sv	vstem –	-	
	Measures for Real Time Systems –				-			
	d Scheduling – Classical uniprocessor			-				
-	RIS tasks – Task assignment – Mode cha				-		-	
0	5	0					0	
UNIT-II	EMBEDDED OS FUNDAMENTAI	S					12 Ho	urs
	Deperating System Fundamentals, Gene		and I	Inix (	OS a	rchitec		
	g Process in Linux GNU Tools: gcc							
	mand line arguments, Make files.	,	Jilditti	onur	com	511411011	, 11 <b>0</b> pi	00005501
	internet internet angementes, truce mes.							
UNIT-III	EMBEDDED C PROGRAMMING						12 Ho	urs
	types –scalar types-Primitive types-En	ume	rated	types-	.suh	ranges		
	-arrays- Functions introduction to E							
-	nterfacing C with Assembly. Emb							-
-	nizing and testing embedded C program		a pro	gram	mig	, 155ue	5 -IC-0	mancy
i ortaonity, Optil	menne and resung entreduced C program	5.						



UNIT-IV	EMBEDDED APPLICATIONS USING DATA P C IA 12 Hours
Linear data str	ructures- Stacks and Queues Implementation of stacks and Queues- Linked List -
	on of linked list, Sorting, Searching, Insertion and Deletion, Nonlinear structures.
1	
UNIT-V	EMBEDDED JAVA 12 Hours
Introduction to	Object Oriented Concepts. Core Java/Java Core- Java buzzwords, Overview of Java
Understanding	Data types, variables and arrays, Operators, Control statements. Embedded Java 3 J2ME,Connected Device configuration, Connected Limited device configuration my of MIDP applications, Advantages of MIDP.
	Total Hours 60 Hours
Text Book(s)	
1.	GNU/Linux application programming, Jones, M Tim, Dream tech press, Ne Delhi.
2.	Embedded / Real-Time Systems : concepts, Design and Programming -The
	Ultimate Reference, Prasad K.V.K.K, Dream tech Press, New Delhi.
3.	Beginning J2ME-From Novice to Professional-3 rd Edition, Sing Li and Jonathan Knudsen, Dreamtech Press, New Delhi
4.	The Complete reference Java2, 5 th Edition, Herbert Schildt, TMH
5.	Data structures Through 'C' Language, Samiran Chattopadhyay, Debarata Ghos Dastidar, Matangini Chattopadhyay, DOEACC Society.
6.	C Programming Language, Kernighan, Brian W, Ritchie, Dennis M, PHI publications.
7.	C and the 8051 Programming Volume II, Building efficient applications, Thomas W Schultz, PHI.
<b>Reference Boo</b>	
1	Unix Network Programming, Stevens, W Richard, PH, New Jersey ACC.NO: B126496
2.	Linux Device Drivers, 2nd Edition, By Alessandro Rubini & Jonathan Corbet, O'Reilly ACC.NO: B65039
3	Data Structures Using C- ISRD group, TMH
4.	Data structures – Seymour Lipschutz, Schaums Outlines
5.	Let us C, Yashwant Kanetkar ACC.NO: B113351
6.	C Programming for Embedded systems, Zurell, Kirk
7.	C and the 8051 Programming for Multitasking – Schultz, Thomas W
8.	C with assembly language, Steven Holzner, BPB publication ACC.NO: B5995
9.	C and the 8051: Hardware, Modular Programming and Multitasking Vol i Schultz, Thomas W
10.	Art of C Programming, Jones, Robin, Stewart, Ian ACC.NO: B56037
11.	Kelley, A & Pohl, I;, " A Book on C", Addison – Wesley
12.	Advanced Linux Programming Mark Mitchell, Jeffrey Oldham, and Alex Samuel, Techmedia.
13.	Embedded/ real-time systems: concepts, design and programming black book, Prasad, K V K K, Dreamtech press, New Delhi. ACC.NO: B127888.



Course Code	T							
Course Name	REAL TIME OPERATING SYSTEM	3	1	0	3	40	60	100
Course		Syllabus Revision V.1						
Category		Synabus Revision V.1.0						
Pre-requisite								
<b>Course Objectiv</b>								
The course shoul	d enable the students -							
	1. To expose the students to the fun	ıdam	nentals	s of i	ntera	iction of	of OS	with a
	computer and User computation.							
	2. To teach the fundamental concepts	of ho	ow pro	ocess	are c	reated a	and con	trolled
	with OS.							
	3. To study on programming logic of	mod	elling	Proce	ess b	ased or	n range	of OS
	features.							
	4. To compare types and Functionalitie							
	5. To discuss the application developm	ent u	ising I	RTOS				
Course Outcom								
<b>.</b>	f the course, the student will be able to							
Course Outcomes	Des	cript	lon					
CO1	Develop knowledge on the operating	SVS	em r	nodell	ing	process	based	on the
001		Develop knowledge on the operating system, modelling process based on the OS and how to develop the application using operating systems.						
CO2	Develop knowledge on the operating	syst	tem, n	nodell	ing	process	based	on the
	OS and how to develop the applicatio	-						
CO3	Develop knowledge on the operating OS and how to develop the applicatio						based	on the
CO4	Develop knowledge on the operating		_				based	on the
	OS and how to develop the application							
CO5	Develop knowledge on the operating				<u> </u>	1		
	OS and how to develop the application	ı usiı	ng RT	OS a	pplic	ation de	omains.	
							10.11	
UNIT-I	REVIEW OF OPERATING SYSTE		11 1		<b>D</b>		12 Ho	
1	- Operating System structures – System						•	
-	of processes – Communication between	-						
	n – issues in distributed system: states,	eve	nts,	clocks	-Dis	tributec	l sched	uling-
Fault & recovery	-							
UNIT-II	RTOS						12 Ho	ours
Real-time concept	pts, Hard Real time and Soft Real-time	, Dif	ferenc	es be	twee	n Gene	ral Purp	oose
OS & RTOS,	Basic architecture of an RTOS,	Sc	heduli	ng S	Syste	ms, Ir	nter-pro	cess
communication,	Performance Matric in scheduling mo	dels	, Inter	rupt	mana	agemen	t in R	ΓOS
environment, Me	emory management. File systems, I/O S	ysten	ns, Ad	lvanta	ge a	nd disa	dvantag	e of
	standards RTOS Issues - Selecting a				-		-	
				-		-		



comparative st	udy.	
UNIT-III	REAL TIME KERNEL	12 Hours
VxWorks Sch	eduling and Task Management - Real-time scheduling, Task	Creation, Intertask
Communicatio	n, Pipes, Semaphore, Message Queue, Signals, Sockets, Interru	pts I/O Systems
General Archi	tecture, Device Driver Studies, Driver Module explanation,	Implementation o
Device Driver	for a peripheral Case study using Vxworks.	
UNIT-IV	REAL TIME MODELS AND LANGUAGES	12 Hours
Event Based -	Process Based and Graph based Models – Real Time Language	s – RTOS Tasks -
	g - Interrupt processing – Synchronization – Control B	
Requirements.		
1		
UNIT-V	RTOS APPLICATION DOMAINS	12 Hours
Case studies-	RTOS for Image Processing – Embedded RTOS for Network	Communication -
	t-Tolerant Applications – RTOS for Control Systems.	
	Total Ho	ours 60 Hours
Text Book(s)		
1.	Silberschatz, Galvin, Gagne "Operating System Concepts Wiley,2003 ACC.NO: B132752.	s", 6th ed, John.
2.	D.M.Dhamdhere," Operating Systems, A Concept-Based App	proch,TMH,2008
3.	Raj Kamal, "Embedded Systems- Architecture, Programming McGraw Hill, 2006. ACC.NO: B133063.	g and Design" Tata
4.	Herma K., "Real Time Systems – Design for distri Applications", Kluwer Academic, 1997.	buted Embedded
5.	Charles Crowley, "Operating Systems-A Design Oriented a Hill,1997.	pproach" McGrav
6.	C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw	Hill, 1997.
7.	Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Re PHI1999.	
8.	Mukesh Sighal and N G Shi "Advanced Concepts in Op McGraw Hill ACC.NO: B132360.	perating System",
9.	VxWorks Programmers Guide.	
).	v x works i rogrammers Ourde.	



<b>Course Code</b>		L	Т	Р	C	IA	EA	TM		
Course Name	SOFTWARE TECHNOLOGY									
	FOR EMBEDDED SYSTEMS	3 1 0 3 40 60								
Course		Syllabus Revision V.1.0								
Category			-							
Pre-requisite										
<b>Course Objectiv</b>										
The course shoul	d enable the students -									
1.	Use of C language for embedded applic	cation	s, con	cepts,	co-de	esign m	ethods.			
Course Outcom	es:									
On completion of	f the course, the student will be able to									
Course	Des	script	tion							
Outcomes		-								
CO1	Develop knowledge in using of Prog	ramm	ing E	mbed	ded S	Systems				
CO2	Develop knowledge in using of C and									
CO3	Develop knowledge in using of Emb				nd So	oftware	Develo	pment		
	Process.		-					-		
CO4	Develop knowledge in using of C la	nguag	ge and	UMI	Lar	iguage	for a re	al time		
	application.									
CO5	Develop knowledge in using of web	archi	tectur	al fra	mewo	ork for	embedd	ed		
	system.									
UNIT-I	PROGRAMMING EMBEDDED S	VSTI	EMS				12 Ho	urs		
	ram – Role of Infinite loop – Compili			r and	10001	ting (				
-		-	-	-		-		_		
	Emulators and simulators processor –	Exter	nai pe	inphe	lai s	- Tope	I OI me	mory		
- Memory testing	g – Flash Memory.									
UNIT-II	C AND ASSEMBLY						12 Ho	ours		
Overview of Em	bedded C - Compilers and Optimization	ı - Pro	ogram	ming	and	Assemb	ly –Res	gister		
	ns – typical use of addressing options		-	-						
-	meter passing – retrieving parameters –			-		-				
variables.	meter passing – retreving parameters –		yunng	5 m pa	100 0	y value	- unp	orar y		
variables.										
UNIT-III	EMBEDDED PROGRAM AND SC	FTV	VADI				12 Ho	11 PG		
UNIT-III	DEVELOPMENT PROCESS	) <u> </u>   V	VANI	2			12 110	ui s		
Program Elemen	ts - Queues - Stack- List and ordered	lists-	- Emb	edded	l prog	grammi	ing in C	C++ -		
-	s and Inline Assembly - Portability				-	-	-			
	ocess: Analysis – Design- Implementat									
Software mainten				0				9		
UNIT-IV	UNIFIED MODELLING LANGUA	AGE					12 Ho age 17 c	urs		
						P	age 17 c	of 58		



Object State Behaviour – UML State charts – Role of Scenarios in the Definition of Behaviour – Timing Diagrams – Sequence Diagrams – Event Hierarchies – Types and Strategies of Operations – Architectural Design in UML Concurrency Design – Representing Tasks – System Task

 Diagram – Concurrent State Diagrams – Threads. Mechanistic Design – Simple Patterns.

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# Course Code WEB ARCHITECTURAL FRAMEWORK FOR 12 Hours EMBEDDED SYSTEM EMBEDDED SYSTEM 12 Hours

Basics – Client/Server model- Domain Names and IP address – Internet Infrastructure and Routing – URL – TCP/IP protocols - Embedded as Web Client - Embedded Web servers - HTML - Web security - Case study: Web-based Home Automation system.

	Total Hours 60 Hours
Text Book(s)	
1.	David E.Simon: "An Embedded Software Primer", Pearson Educat ion, 2003 ACC.NO: B102775.
2.	Michael Barr, "Programming Embedded Systems in C and C++" Oreilly, 2003.
3.	H.M. Deitel, P.J.Deitel, A.B. Golldberg "Internet a nd World Wide Web – How to Program" Third Edition, Pearson Education, 2001. ACC.NO: B111693.
4.	Bruce Powel Douglas, "Real-Time UML, Second Edition: Developing Efficient Object for Embedded Systems, 2nd edition ,1999, Addison-Wesley.
5.	Daniel W.lewis "Fundamentals of Embedded Software where C and Assembly meet" PHI 2002. ACC.NO: B100506.
6.	Raj Kamal, "Embedded Systems- Architecture, Programming and Design" TMH, 2006. ACC.NO: B133063.



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Course Name	EMBEDDED NETWORKING											
		3	1	0	3	40	60	100				
Comme			C. P. Y	P								
Course Category			Syllal	dus R	evisi	on	V.1.0					
Pre-requisite												
Course Objectiv	es:											
	l enable the students -											
1.	To impart knowledge on Serial and part	alle	l comr	nunica	ation	protoc	ols					
2.	Application Development using USB a	und (	CAN b	ous for	PIC	micro	controll	ers				
3.	Application development using Embed	lded	Ethern	net for	Rat	bit pro	cessors.	Wireless sensor				
	network communication protocols.					-						
Course Outcome	28:											
On completion of	the course, the student will be able to											
Course		D	escrip	otion								
Outcomes												
<u>CO1</u>	Develop knowledge in the protocols,			comn	nunio	cation p	orotocol	S.				
<u>CO2</u>	Develop knowledge in USB and CAN											
<u>CO3</u>	Develop knowledge in controller area											
<u>CO4</u>	Develop knowledge in embedded eth			~ "l	- mal	atad an	mliantia					
CO5	Develop knowledge in wireless embe	aaec	1 netw	orking	g rei	ated ap	pricatio	<u>n.</u>				
							r					
UNIT-I	EMBEDDED COMMUNICATION	PR(	отос	OLS			12 Ho	urs				
					eri al	comm						
Embedded Netwo	orking: Introduction–Serial / Parallel Co	mm	unicati	ion-S			unicatio	on protocols -RS232				
Embedded Netwo standard – RS485	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri	mm al Pe	unicati eriphei	ion–So ral Int	erfac		unicatio	on protocols -RS232				
Embedded Netwo standard – RS485	orking: Introduction–Serial / Parallel Co	mm al Pe	unicati eriphei	ion–So ral Int	erfac		unicatio	on protocols -RS232				
Embedded Netwo standard – RS485 (I2C) – PC Paralle	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot	mm al Pe	unicati eriphei	ion–So ral Int	erfac		unication ) – Inter	on protocols -RS232 r Integrated Circuits				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS	mm al Pe ocol	unicati eripher s – Fir	ion–So ral Int rewire	erfac	ce (SPI)	unicatio ) – Inter 12 Ho	on protocols -RS232 r Integrated Circuits <b>urs</b>				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on	mm al Pe ocol	unicati eripher s – Fir bus	ion–Seral Int rewire	erfac B St	ates –	unicatio ) – Inter 12 Ho	on protocols -RS232 r Integrated Circuits <b>urs</b>				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI	mm al Pe ocol the C 1	unicati eripher s – Fir bus – 8 Mic	ion–So ral Int ewire – USI rocon	erfac B St trolle	ete (SPI) ates – er	unicatio ) – Inter <b>12 Ho</b> USB bu	on protocols -RS232 r Integrated Circuits ours communication:				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction -	mm al Pe ocol the C 1 Fran	unicati eripher s – Fir bus 8 Mic nes –B	ion–So ral Int rewire – USI rocon	erfac	ates – er g –Type	unicatio ) – Inter <b>12 Ho</b> USB bu es of err	on protocols -RS232 r Integrated Circuits ours communication:				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI	mm al Pe ocol the C 1 Fran	unicati eripher s – Fir bus 8 Mic nes –B	ion–So ral Int rewire – USI rocon	erfac	ates – er g –Type	unicatio ) – Inter <b>12 Ho</b> USB bu es of err	on protocols -RS232 r Integrated Circuits ours communication:				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac	mm al Pa ocol the C 1 Fran e –A	unicati eripher s – Fir bus 8 Mic nes –B	ion–So ral Int rewire – USI rocon	erfac	ates – er g –Type	unicatio ) – Inter <b>12 Ho</b> USB bu es of ern n CAN.	on protocols -RS232 r Integrated Circuits ours communication:				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac	mmu al Pe ocol the C 1 Fran e –A	unicati eripher s – Fir bus 8 Mic 8 Mic anes –B simpl	ion—So ral Int ewire – USI rocon Sit stu le app	erfac	ates – er g –Type	unicatio ) – Inter <b>12 Ho</b> USB bu es of err n CAN. <b>12 Ho</b>	on protocols -RS232 r Integrated Circuits ours communication: cors –				
Embedded Netwo standard – RS485 (I2C) – PC Parall UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac CONTROLLER AREA NETWORK Network – Underlying Technology, C.	mm al Pe ocol the C 1 Fran e – A	unicati eripher s – Fir bus – 8 Mic: nes –B a simpl	ion—So ral Int rewire – USI rocon Bit stu le app	erfac B St trolle uffing licati	ates – er g –Type ion with ecting	unicatio ) – Inter <b>12 Ho</b> USB bu es of ern n CAN. <b>12 Ho</b> a CAN	on protocols -RS232 r Integrated Circuits ours communication: cors – controller – CAN				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area I development too	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac CONTROLLER AREA NETWORK Network – Underlying Technology, C. ls. Implementing CAN open Commu	mm al Pe ocol the C 1 Fran e –A K AN	unicati eripher s – Fir bus – 8 Mic 8 Mic nes –B simpl Overv tion 1	ion—So ral Int ewire – USI rocon Sit stu le app riew – ayout	erfac B St trolle licati licati	ates – er g –Type ion with ecting l requi	unicatio ) – Inter <b>12 Ho</b> USB bu es of err n CAN. <b>12 Ho</b> a CAN rements	on protocols -RS232 r Integrated Circuits ours communication: cors – ours Controller – CAN s – Comparison of				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area I development too implementation n	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac CONTROLLER AREA NETWORK Network – Underlying Technology, C.	mm al Pe ocol the C 1 Fran e –A K AN	unicati eripher s – Fir bus – 8 Mic 8 Mic nes –B simpl Overv tion 1	ion—So ral Int ewire – USI rocon Sit stu le app riew – ayout	erfac B St trolle licati licati	ates – er g –Type ion with ecting l requi	unicatio ) – Inter <b>12 Ho</b> USB bu es of err n CAN. <b>12 Ho</b> a CAN rements	on protocols -RS232 r Integrated Circuits ours communication: cors – ours Controller – CAN s – Comparison of				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area I development too	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac CONTROLLER AREA NETWORK Network – Underlying Technology, C. ls. Implementing CAN open Commu	mm al Pe ocol the C 1 Fran e –A K AN	unicati eripher s – Fir bus – 8 Mic 8 Mic nes –B simpl Overv tion 1	ion—So ral Int ewire – USI rocon Sit stu le app riew – ayout	erfac B St trolle licati licati	ates – er g –Type ion with ecting l requi	unicatio ) – Inter <b>12 Ho</b> USB bu es of err n CAN. <b>12 Ho</b> a CAN rements	on protocols -RS232 r Integrated Circuits ours communication: cors – ours Controller – CAN s – Comparison of				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area I development too implementation n cycle.	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac CONTROLLER AREA NETWORK Network – Underlying Technology, C. Is. Implementing CAN open Commu- nethods – Micro CAN open – CAN open	mm al Pe ocol the C 1 Fran e –A K AN	unicati eripher s – Fir bus – 8 Mic 8 Mic nes –B simpl Overv tion 1	ion—So ral Int ewire – USI rocon Sit stu le app riew – ayout	erfac B St trolle licati licati	ates – er g –Type ion with ecting l requi	unicatio ) – Inter <b>12 Ho</b> USB bu es of err n CAN. <b>12 Ho</b> a CAN rements nce test	on protocols -RS232 r Integrated Circuits ours is communication: fors – fors – fors – fors – fors – fors – for for a comparison of for a comparison of for a comparison of for a comparison of for a compariso				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area I development too implementation n cycle.	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac CONTROLLER AREA NETWORK Network – Underlying Technology, C. ls. Implementing CAN open Communethods – Micro CAN open – CAN open	mmu al Pe ocol the C 1 Fran e –A X AN mica en so	unicati eripher s – Fir bus – 8 Mic: nes –B simpl Overv tion 1 ource c	ion—So ral Int ewire – USI rocom Sit stu le app riew – ayout code –	erfac B St trolle uffing licati - Sel and - Con	e (SPI) ates – er g –Typo on with ecting l requi	unicatio ) – Inter <b>12 Ho</b> USB bu es of ern n CAN. <b>12 Ho</b> a CAN rements nce test	on protocols -RS232 r Integrated Circuits ours is communication: fors – fours Controller – CAN s – Comparison of – Entire design life				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area I development too implementation n cycle.	orking: Introduction–Serial / Parallel Co         5 – Synchronous Serial Protocols - Seri         el port programming -ISA/PCI Bus prot <b>USB AND CAN BUS</b> troduction – Speed Identification on         w types –Enumeration –Descriptors –PI         C Programs –CAN Bus – Introduction -         ing – PIC microcontroller CAN Interfac <b>CONTROLLER AREA NETWORF</b> Network – Underlying Technology, C.         ls. Implementing CAN open Communethods – Micro CAN open – CAN open <b>EMBEDDED ETHERNET</b> ages using UDP and TCP – Serving w	mmu al Pe ocol the C 1 Fran e – A K AN unica en so	unicati eripher s – Fir bus – 8 Mic 8 Mic anes –B a simpl Overv tion 1 ource o	ion—So ral Int ewire – USI rocon bit stu le app iew – ayout code –	B St trolle uffing licati - Sel and - Con	ates – er g –Type ion with ecting l requi- nformar	unicatio ) – Inter <b>12 Ho</b> USB bu es of err n CAN. <b>12 Ho</b> a CAN rements nce test <b>12 Ho</b> ta – Se	on protocols -RS232 r Integrated Circuits ours is communication: fors – fours Controller – CAN is – Comparison of – Entire design life				
Embedded Netwo standard – RS485 (I2C) – PC Paralle UNIT-II USB bus – Int Packets –Data flo USB Interface – C Nominal Bit Timi UNIT-III Controller Area I development too implementation n cycle.	orking: Introduction–Serial / Parallel Co 5 – Synchronous Serial Protocols - Seri el port programming -ISA/PCI Bus prot USB AND CAN BUS troduction – Speed Identification on w types –Enumeration –Descriptors –PI C Programs –CAN Bus – Introduction - ing – PIC microcontroller CAN Interfac CONTROLLER AREA NETWORK Network – Underlying Technology, C. ls. Implementing CAN open Communethods – Micro CAN open – CAN open	mmu al Pe ocol the C 1 Fran e – A K AN unica en so	unicati eripher s – Fir bus – 8 Mic 8 Mic anes –B a simpl Overv tion 1 ource o	ion—So ral Int ewire – USI rocon bit stu le app iew – ayout code –	B St trolle uffing licati - Sel and - Con	ates – er g –Type ion with ecting l requi- nformar	unicatio ) – Inter <b>12 Ho</b> USB bu es of err n CAN. <b>12 Ho</b> a CAN rements nce test <b>12 Ho</b> ta – Se	on protocols -RS232 r Integrated Circuits ours is communication: fors – fours Controller – CAN is – Comparison of – Entire design life				



UNIT-V	WIRELESS EMBEDDED NETWORKING 12 Hours						
Wireless sensor networks – Introduction – Applications – Network Topology – Localization –							
Synchronization - Energy efficient MAC protocols -SMAC - Energy Efficient and robust routing - Data Ce							
routing.							
	Total Hours 60 Hours						
Text Book(s)							
1.	Frank Vahid, Givargis 'Embedded Systems Design: A Unified Hardware/ Software						
	Introduction', Wiley Publications						
2.	Jan Axelson, 'Parallel Port Complete', Penram publications.						
3.	Dogan Ibrahim, 'Advanced PIC microcontroller projects in C', Elsevier 2008.						
4.	Jan Axelson 'Embedded Ethernet and Internet Complete', Penram publications.						
5.	Bhaskar Krishnamachari, 'Networking wireless sensors', Cambridge press, 2005.						
6.	Glaf P.Feiffer, Andrew Ayre and Christian Keyold, "Embedded networking with CAN and						
	CAN open", Embedded System Academy 2005.						



Course Code		L	Т	Р	С	IA	EA	TM
Course Name	EMBEDDED COMMUNICATION SOFTWARE DESIGN	3	1	0	3	40	60	100
Course			Sylla	bus R	levisi	on	V.	1.0
Category								
Pre-requisite								
Course Objectiv	ves: ld enable the students -							
	To know about the OSI Model for H	Embedd	ed Co	mmu	nicati	on		
	To know about the software design					011.		
2.	To know about the software design		comm	luinea				
Course Outcom	es: f the course, the student will be able t	0						
Course		escript	ion					
Outcomes		1						
CO1	Develop knowledge and understa model.	nding t	he va	rious	aspe	cts of	OSI ref	erence
CO2	Develop knowledge and unders partitioning.	tanding	the	vario	ous a	spects	of so	ftware
CO3	Develop knowledge and understar structures.	nding th	e vari	ous a	spect	s tables	s & oth	er data
CO4	Develop knowledge and understa software.	anding	the v	arious	s asp	ects of	i manag	gement
C05	Develop knowledge and underst communication software design.	anding	the v	variou	s asp	ects o	f multi	board
UNIT-I	OSI REFERENCE MODEL						12 Ho	urs
	n Devices – Communication Echo Sy n – Embedded Communication Syster		-		nside	ration -	– Host I	Based
UNIT-II	SOFTWARE PARTITIONING						12 Ho	urs
	trict Layering – Tasks & Modules – er3 Switch / Routers – Protocol						tion –La	ayer2
				011			51	
Switch – Lay							12 Ho	
Switch – Lay Debugging Pro UNIT-III	tocols. TABLES & OTHER DATA STR	UCTUI	RES				12 Ho	ours
Switch – Lay Debugging Pro UNIT-III Partitioning of	tocols.	UCTUI on – Sp	<b>RES</b> eeding	g Up a	acces	s – Tab	12 Ho le Resiz	ours
Switch – Lay Debugging Pro UNIT-III Partitioning of	tocols. <b>TABLES &amp; OTHER DATA STR</b> Structures and Tables – Implementation	UCTUI on – Sp	<b>RES</b> eeding	g Up a	acces	s – Tab	12 Ho le Resiz	ours zing
Switch – Lay Debugging Pro UNIT-III Partitioning of – Table access UNIT-IV	tocols. TABLES & OTHER DATA STR Structures and Tables – Implementation routines – Buffer and Timer Managen	UCTUI on – Sp nent – T	RES eedin; Third 1	g Up a Party 1	access Proto	s – Tab col Lib	12 Ho de Resiz praries.	zing



UNIT-V	MULTI BOARD COMMUNICATION SOFTWARE	12 Hours
	DESIGN	
Multi Board A	Architecture – Single control Card and Multiple line C and Architectur	re –Interface
for Multi Boa	rd software - Failures and Fault - Tolerance in Multi Board Systems	– Hardware
indonondont d		4 TT 1
independent d	evelopment – Using a COTS Board – Development Environment – Te	est 100ls.
independent d	evelopment – Using a COTS Board – Development Environment – Te	est 1 ools.
	Total Hours	60 Hours
*		
<b>x</b>		60 Hours
<b>x</b>	Total Hours	60 Hours
Text Book(s) 1. 2.	Total Hours Sridhar .T, "Designing Embedded Communication Software" CMI	<b>60 Hours</b> P Books,



Course Code		L	Т	Р	С	IA	EA	ТМ		
Course	EMBEDDED SYSTEMS LABORATORY	3	1	0	3	40	60	100		
Name		3	1	0	3	40	00	100		
Course		Syllabus Revision V.1.0								
Category Pre-										
requisite										
Course Ob	iectives:									
	should enable the students -									
	1. To design 8051,PIC and 16 bit process	sors	for 1	l/O pr	ogra	mmi	ng, se	rial port		
	programming for PWM generation, me	otor	cont	rol, I	LCD	, RT	C and	Sensor		
	interfacing.									
	2. To design and analyse wired/wireless ne	twor	ks us	sing N	S2 s	imula	ator.			
Course Out										
_	ion of the course, the student will be able to									
Course	Descripti	ion								
Outcomes	Desiry 9 Lit Misses extra llars									
CO1 CO2	Design 8-bit Microcontrollers.									
CO2 CO3	Design 16-bit Microcontrollers.									
CO3 CO4	Design ARM Processor. Design Xilinx/Altera FPGA and CPLD.									
C04 C05	Design Network Simulators.									
005	Design Network Simulators.									
	LIST OF EXPERIMENTS									
1. Desig	gn with 8 bit Microcontrollers 8051/PIC Microc	ontro	ollers	5.						
i)I/O	Programming, Timers, Interrupts, Serial port p	rogra	amm	ing.						
ii) F	WM Generation, Motor Control, ADC/DAC	, L	CD a	and R	TC	Inter	facing	, Sensor		
Inter	facing.									
iii) B	oth Assembly and C programming.									
	gn with 16 bit processors. I/O programming, Tir	mers	Inte	errupts	, Sei	rial C	ommu	nication.		
3. Desi	gn with ARM Processors. I/O programming, AI	DC/E	AC,	Time	rs, Ir	nterru	pts.			
4. Study	y of one type of Real Time Operating Systems (	RTO	S).		ŕ		1			
-	ronic Circuit Design of sequential, combination		<i>,</i>	circui	ts us	ing (	CAD T	ools.		
	lation of digital controllers using MATLAB/La		•			0				
	ramming with DSP processors for Correlation			volutio	n. /	Arithr	netic	adder.		
U	ier, Design of Filters - FIR based IIR based.	-,			, 1		•			
-	gn with Programmable Logic Devices using Xil	inx/4	Alter	a FPG	A ar	nd CP	'LD			
	gn and Implementation of simple Combinationa						<i></i> ,			
	ork Simulators Simple wired/ wireless network		-							
	ramming of TCP/IP protocol stack.	51110		JII USII.	15 IN	54.				
11.1106										
				Tota	l He	ours	60 H	ours		



Course		L	Т	Р	С	IA	EA	ТМ		
Code	ADVANCED DIGITAL SIGNAL									
Course Name	PROCESSING	3	1	0	3	40	60	100		
Course		Syllabus Revision V.1.0								
Category										
Pre-										
requisite										
Course Ob										
The course	should enable the students -	6 D	an	1 ·		c 1 [.]	• •			
	1. To make the student learn: theory of			-		-	sital s	ignal		
	processing applications and an introduct	.10n t	to D	SP pro	cess	ors.				
Course Ou										
	ion of the course, the student will be able to									
Course	Description	a								
Outcomes	Davalan knowladge of digerate random gignal		1	ha and	had	dad a	vatam			
CO1 CO2	Develop knowledge of discrete random signal Develop knowledge of estimation and p									
02	embedded system.	reure		teem	inqu	es us	seu II	i the		
CO3	Develop knowledge of digital signal process	or us	ed in	n the e	mhe	dded	syste	m		
CO3	Develop knowledge of application of VLSI									
001	the embedded system.	mpi	UIIIU		1 000		ues us	<b>vu</b> 111		
CO5	Develop knowledge of VLSI implementation	usec	l in t	he em	beda	led s	ystem.			
							,			
UNIT-I	DISCRETE RANDOM SIGNAL						12H	ours		
Discrete Ra	indom Processing – Expectations – Variance	- Ca	o-Va	riance	; – S	Scala	Prod	luct –		
	Discrete Signals – Parseval's Theorem – Wie									
	ensity – Periodogram. Autocorrelation – Sum I									
-	n Theorem – Discrete Random Signal Processi		-				-			
	bise – Low Pass Filtering of White Noise.	05	<i>,</i>		<i></i>	-				
UNIT-II	ESTIMATION AND PREDICTION TECH	ΙΝΙς	<b>)UE</b>	S			12H	ours		
Discrete Ra	ndom Processes – Ensemble averages, Stationa	iry p	roce	sses, A	Auto	corre	lation	and		
	riance matrices. Parseval's Theorem, Wiene									
	nsity . AR, MA, ARMA model based spectral									
-	iction – Forward and backward predictions, Le									
-	er for filtering and prediction, Discrete Kalman			~ 1 ~ ~ 1						
,, 101101 11110			•							
UNIT-III	DIGITAL SIGNAL PROCESSOR						1211	ours		
-		1.4		D	A	1.2				
Basic Are	Basic Architecture – Computational building blocks, MAC, Bus Arc hitecture and									

Basic Architecture – Computational building blocks, MAC, Bus Arc hitecture and memory, Data Addressing, Parallelism and pipelining, Parallel I/O interface, Memory Interface, Interrupt, DMA.



UNIT-IV	APPLICATION OF VLSI IMPLEMENTATION	12Hours
Basics on	DSP system architecture design using VHDL programming, Mappin	g of DSP
algorithm	onto hardware, Realization of MAC & Filter structure.	
UNIT-V	VLSI IMPLEMENTATION	12Hours
	DSP system architecture design using VHDL programming, Mappin onto hardware, Realization of MAC & Filter structure.	g of DSP
	Total Hours	60Hours
Text Book	(s)	
1.	Bernard Widrow, Samuel D. Stearns, "Adaptive Signal Processing" Education, third edition, 2004. ACC.NO: B130380.	, Pearson
2.	Dionitris G. Manolakis, Vinay K. Ingle, Stepen M. Kogon,"Sta Adaptive signal processing, spectral estimation, signal modeling, filtering & Array processing", McGraw-Hill International edition 2000	Adaptive
3.	Monson H. Hayes, "Statistical Digital Signal Processing and Modelli Wiley and Sons, Inc.,	
4.	John G. Proaks, Dimitris G. Manolakis, "Digital Signal Pr ocessing Education 2002.	g", Pearson
5.	S. Salivahanan, A. Vallavaraj and C. Gnanapriya "Digital Signal P TMH,2000. ACC.NO: B124703	rocessing",
6.	Avatar Sing, S. Srinivasan, "Digital Signal Processing- Implementa DSP Microprocessors with Examples from TMS320C54xx", Thon 2004.	-
7.	Lars Wanhammer, "DSP Integrated Circuits", Academic pres s, 1999,	
8.	Ashok Ambardar,"Digital Signal Processing: A Modern Introduction" India edition, 2007.	•
9.	Lars Wanhammer, "DSP Integrated Circuits", Academic pres s, 1999,	New York.



Course Code		L	Т	Р	С	IA	EA	ТМ	
Course	RISC PROCESSOR ARCHITECTURE								
Name	AND PROGRAMMING	3	1	0	3	40	60	100	
Course	Syllabus Revision								
Category									
Pre-									
requisite									
Course Ob									
The course	should enable the students -								
	1. To teach the architecture of 8 bit RISC p				ra a				
	2. To teach the architecture and programm					proce	ssor.		
	3. To teach the implementation of DSP in		-						
	4. To discuss on memory management in I								
	5. To teach the application development w	rith A	RM	proce	ssor				
Course Ou	tcomes·								
	ion of the course, the student will be able to								
Course	Description	n							
Outcomes									
CO1	Develop knowledge in AVR microc implementation in various field.	ontro	oller	arch	itect	ure	and	their	
CO2	Develop knowledge in 8 and 16 bit RISC provarious field.	ocess	or ar	nd the	ir im	plem	entati	on in	
CO3	Develop knowledge in ARM application dev in various field.	elop	ment	and t	heir	impl	ement	ation	
CO4	Develop knowledge in memory protecti implementation in various field.	on	and	mana	agen	nent	and	their	
CO5	• · · · · · · · · · · · · · · · · · · ·	arm	mic	rocon	troll	ers	and	their	
	I								
UNIT-I	AVR MICROCONTROLLER ARCHITE				<b></b>			ours	
	re – memory organization – addressing modes			-					
	RAM –Timer –UART – Interrupt Structure- S	Seria	I Co	mmur	iicati	on w	vith P	C —	
ADC/DAC	C Interfacing.								
UNIT-II	ARM ARCHITECTURE AND PROGRAM	4MI	NG				12H	ours	
Arcon RI	SC Machine – Architectural Inheritance – C			Archit	ectur	es. 7			
	er's model -Registers – Pipeline - Interrup					-			
-	family – Co-processors. Instruction set – Th				-				
cycle timi		anno	mst	1 40110	11 50	ι I	iisti ut	1011	
	ugs.								
UNIT-III	ARM APPLICATION DEVELOPMENT						12H	ours	
Introductio	on to DSP on ARM –FIR Filter – IIR Filte	r – 1	Disci	rete F	ouri	er tra	insfor	m –	



Exception Handling – Interrupts – Interrupt handling schemes- Firmware and bootloader – Example: Standalone - Embedded Operating Systems – Fundamental Components -Example Simple little Operating System.

#### UNIT-IV MEMORY PROTECTION AND MANAGEMENT

**12Hours** 

Protected Regions-Initializing MPU, Cache and Write Buffer-MPU to MMU-Virtual Memory-Page Tables-TLB-Domain and Memory Access Permission-Fast Context Switch Extension.

UNIT-V	DESIGN WITH ARM MICROCONTROLLERS	12Hours				
Assembler	Assembler Rules and Directives- Simple ASM/C programs- Hamming Code- Division-					
Negation-	Simple Loops –Look up table- Block copy- subroutines.					
	Total Hours	60Hours				
Text Book(	s)					
1.	Steve Furber, 'ARM system on chip architecture', Addision Wesley.					
2.	Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield 'AF	RM System				
	Developer's Guide Designing and Optimizing System Software', Else	vier 2007.				
3.	Trevor Martin, 'The Insider's Guide To The Philips AR	M7-Based				
	Microcontrollers, An Engineer's Introduction To The LPC2100 Ser	ies' Hitex				
	(UK) Ltd.,					
4.	Dananjay V. Gadre 'Programming and Customizing the AVR microco	ntroller',				
	McGraw Hill 2001.					
5.	William Hohl, 'ARM Assembly Language' Fundamentals and Techni	ques.				
6.	ARM Architecture Reference Manual.					
7.	LPC213x User Manual.					



## SYLLABUS (2023-24) M.E (EMBEDDED SYSTEM TECHNOLOGIES)

		L	Т	Р	С	IA	EA	ТМ	
Code				1		IA	ĽA	1 191	
Course	WIRELESS AND MOBILE	2	1	0	2	10	(0)	100	
Name	COMMUNICATION	3	1	0	3	40	60	100	
Course	Syllabus Revision V.1.0								
Category									
Pre-									
requisite									
Course Ob The course	<ul> <li>should enable the students -</li> <li>1. To expose the students to the fundamentation technologies.</li> <li>2. To teach the fundamentals of wireless</li> <li>3. To study on wireless network topologies.</li> <li>4. To introduce network routing protocol</li> </ul>	mob ies.						ion	
	4. To introduce network routing protocol	15.							
Course Ou	tcomes:								
	tion of the course, the student will be able to								
Course	Descript	ion							
Outcomes									
CO1	Develop knowledge in the basic of technologi							ftware.	
CO2	Develop knowledge in the basic of technologi			obile 1	netw	orks.			
<u>CO3</u>	Develop knowledge in the basic of wireless no	etwo	rks.						
<u>CO4</u>	Develop knowledge in the basic of routing.								
CO5	Develop knowledge in the basic of transport a	ind a	pplic	cation	laye	rs.			
UNIT-I	INTRODUCTION						12 H	lours	
	ransmission – signal propagation – Free space a	and t	wo r	av mo	dele	_ cn			
	ansinission – signai propagation – rice space a			-		– sp	icau s	peculum	
	tworks Consoity Allocation EDMA TDMA	CDV	<i>Γ</i> ΛΤ	<b>\</b> \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	1				
	etworks – Capacity Allocation – FDMA–TDMA-	SDN	IA-I	DAMA	<b>\</b> .				
Satellite Ne		SDN	IA-I	DAMA	A.		12 H	lours	
Satellite Ne	MOBILE NETWORKS					ion F		lours shment -	
Satellite Ne UNIT-II Cellular W	MOBILE NETWORKS ireless Networks – GSM – Architecture – Pr					ion E			
Satellite Ne UNIT-II Cellular W	MOBILE NETWORKS					ion E			
Satellite Ne UNIT-II Cellular W Frequency	MOBILE NETWORKS ireless Networks – GSM – Architecture – Pr Allocation – Handover – Security – GPRS.					ion E	Establi	shment -	
Satellite Ne UNIT-II Cellular W Frequency UNIT-III	MOBILE NETWORKS ireless Networks – GSM – Architecture – Pr Allocation – Handover – Security – GPRS. WIRELESS NETWORKS	otoco	ols -	- Con	necti		Establi 12 H		
Satellite Ne UNIT-II Cellular W Frequency UNIT-III	MOBILE NETWORKS ireless Networks – GSM – Architecture – Pr Allocation – Handover – Security – GPRS.	otoco	ols -	- Con	necti		Establi 12 H	shment -	
Satellite Ne UNIT-II Cellular W Frequency UNIT-III	MOBILE NETWORKS ireless Networks – GSM – Architecture – Pr Allocation – Handover – Security – GPRS. WIRELESS NETWORKS	otoco	ols -	- Con	necti		Establi 12 H etooth	shment -	
Satellite Ne UNIT-II Cellular W Frequency UNIT-III Wireless L UNIT-IV	MOBILE NETWORKS ireless Networks – GSM – Architecture – Pr Allocation – Handover – Security – GPRS. WIRELESS NETWORKS AN – IEEE 802.11 Standard-Architecture – Ser	otoco	ols - s – H	- Con	necti	Blue	Establi 12 H etooth 12 H	shment - lours	



UNIT-V	TRANSPORT AND APPLICATION LAYERS	12 Hours					
TCP over	TCP over Adhoc Networks - WAP - Architecture - WWW Programming Model - WDP -						
WTLS -	WTLS – WTP – WSP – WAE – WTA Architecture – WML – WML scripts.						
	Total Hours	60 Hours					
<b>Text Book</b>	(s)						
1.	Kaveh Pahlavan, Prasanth Krishnamoorthy, "Principles of Wireles s	Networks'					
	PHI/Pearson Education, 2003 ACC.NO: B122027.						
2.	C. Siva Ram Murthy and B.S. Manoj, Adhoc Wireless Networks: An	rchitectures and					
	protocols, Prentice Hall PTR, 2004						
3.	Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober	, "Principles of					
	Mobile computing", Springer, New york, 2003. ACC.NO: B129477.						
4.	C.K.Toh, "AdHoc mobile wireless networks", Prentice Hal I, Inc, 2002						
5.	Charles E. Perkins, "Adhoc Networking", Addison-Wesley, 2001.						
6.	Jochen Schiller, "Mobile communications", PHI/Pearson Educati on,	Second Edition,					
	2003 ACC.NO: B132742.						
7.	William Stallings, "Wireless communications and Networks", PHI/Pea	rson Education,					
	2002.						



Course Code		L	Т	Р	С	IA	EA	ТМ	
Course Name	BIG DATA ANALYTICS	3	1	0	3	40	60	100	
Course		Syllabus Revision V.1.0							
Category									
Pre- requisite									
requisite Course Objectives:									
Course Objectives: The course should enable the students -									
1110 000000		is the	next wa	ave for	r busine	esses lo	oking	for	
	<ol> <li>To understand big data analytics as the next wave for businesses looking for competitive advantage.</li> </ol>								
	2. To understand the financial value	of big	data a	nalytic	cs.				
	3. To explore tools and practices for	-		-					
	4. To understand how big data analy		-	-		v com	oonent		
	5. To understand how to mine the da			0:		, <u>-</u> ]			
	<ol> <li>6. To learn about stream computing.</li> </ol>								
	<ol> <li>To hear about shear comparing.</li> <li>To know about the research that research th</li></ol>		s the in	tegrat	ion of I	arge a	nounts	of	
	data.	- 1 - 1		Or at					
Course Ou	tcomes:								
	ion of the course, the student will be able	to							
Course		script	ion						
Outcomes									
C01	Identify the need for big data analytics f								
CO2	Identify the need for Data analysis for a	doma	in.	<u> </u>	<u> </u>			11 /	
CO3	Contextually integrate and correlate la	rge ar	nounts	of in	tormati	on aut	omatica	ally to	
CO4	gain faster insights. Suggest areas to apply big data to increa	se hu	iness o	utcor	10				
C04 C05	Use Hadoop, Map Reduce Framework					r a oiv	en nrol	lem	
0.05	ose madoop, map reduce i namework i	ippiy	oig uu	a anai	<u>yties 10</u>	1 4 51		/10111.	
UNIT-I	INTRODUCTION TO BIG DATA						12 Ho	urs	
Analytics -	Nuances of big data - Value - Issues -	- Case	e for Bi	ig data	a – Big	data	options	Team	
challenge -	Big data sources - Acquisition - Nuts a	and B	olts of	Big da	ata. Fea	tures	of Big	Data -	
-	ompliance, auditing and protection - Evol			-			-		
	Big data characteristics - Volume, Vera								
	tools – Green plum – Informatics.		-		-				
-	*								
UNIT-II	DATA ANALYSIS						12 Ho	urs	
Evolution	of analytic scalability – Convergence – p	aralle	l proces	ssing s	ystems	- Clo	ud com	puting	
– grid cor	nputing – map reduce – enterprise analy	ytic sa	and box	x – an	alytic d	lata se	ts – Ai	nalytic	
-	- analytic tools – Cognos – Microstrategy				-			-	
	ce – business approaches – Analytic innov			-					
UNIT-III	STREAM COMPUTING						12 Ho	urs	
L	L								



Introduction to Streams Concepts – Stream data model and architecture - Stream Computing, Sampling data in a stream – Filtering streams – Counting distinct elements in a stream – Estimating moments – Counting oneness in a window – Decaying window - Real time Analytics Platform (RTAP) applications IBM Infosphere – Big data at rest – Infosphere streams – Data stage – Statistical analysis – Intelligent scheduler – Infosphere Streams.

#### UNIT-IV PREDICTIVE ANALYTICS AND VISUALIZATION

12 Hours

Predictive Analytics – Supervised – Unsupervised learning – Neural networks – Kohonen models – Normal – Deviations from normal patterns – Normal behaviours – Expert options – Variable entry - Mining Frequent item sets - Market based model – A priori Algorithm – Handling large data sets in Main memory – Limited Pass algorithm – Counting frequent item sets in a stream – Clustering Techniques – Hierarchical– K-Means – Clustering high dimensional data Visualizations -Visual data analysis techniques, interaction techniques; Systems and applications.

#### UNIT-V FRAMEWORKS AND APPLICATIONS

12 Hours

IBM for Big Data – Map Reduce Framework - Hadoop – Hive – Sharding – NoSQL Databases - S3 - Hadoop Distributed file systems – Hbase – Impala – Analyzing big data with twitter – Big data for ECommerce – Big data for blogs.

Total Hours 60 Hours

Text Book	(\$)
1	Frank J Ohlhorst, "Big Data Analytics: Turning Big Data into Big Money", Wiley
	and SAS Business Series, 2012.
2.	Colleen Mccue, "Data Mining and Predictive Analysis: Intelligence Gathering and
	Crime Analysis", Elsevier, 2007
3.	Michael Berthold, David J. Hand, Intelligent Data Analysis, Springer, 2007.
4.	Anand Rajaraman and Jeffrey David Ullman, Mining of Massive Datasets,
	Cambridge University Press, 2012.
5.	Bill Franks, "Taming the Big Data Tidal Wave: Finding Opport unities in Huge
	Data Streams with Advanced Analytics", Wiley and SAS Business Series, 2012.
6.	Paul Zikopoulos, Chris Eaton, Paul Zikopoulos, "Understanding Big Data : Analytics
	for Enterprise Class Hadoop and Streaming Data", McGraw Hill, 2011.
7.	Paul Zikopoulos, Dirk deRoos, Krishnan Parasuraman, Thomas Deutsch , James
	Giles, David Corrigan, "Harness the Power of Big data – The big data plat form",
	McGraw Hill, 2012.
8.	Glenn J. Myatt, Making Sense of Data, John Wiley & Sons, 2007
9.	Pete Warden, Big Data Glossary, O'Reilly, 2011.
10.	Jiawei Han, Micheline Kamber "Data Mining Concepts and Techniques", Second
	Edition, Elsevier, Reprinted 2008.





Code course Name       ASIC DESIGN       3       1       0       3       40       60       100         Course Name       ASIC DESIGN       3       1       0       3       40       60       100         Course Name       Syllabus Revision       V.1.0       V.1.0       V.1.0         Course Objectives:       The course objectives:       V.1.0       V.1.0         The course objectives:       To Develop knowledge in basic transistor logic.       2.       To Develop knowledge in various programming platform like Altera, Xilinx.         Course Outcomes:       Description       Outcomes       Ocourse       Ocourse         Outcomes       Develop knowledge in Introduction TO ASICS, CMOS Logic and ASIC Library Design.       Develop knowledge in programmable ASIC s, programmable ASIC logic cells and programmable ASIC I/O cells.         CO3       Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.       12       Hours         CO4       Develop knowledge in ASIC construction, floor planning, placement and routing.       12       Hours         UNIT-I       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC       12       Hours         Library Design       Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resist	Course		L	Т	Р	С	IA	EA	ТМ	
Name       ASIC DESIGN       3       1       0       3       40       60       100         Course Category       Syllabus Revision       V.1.0         Pre- requisite       Syllabus Revision       V.1.0         Course Objectives:       1.       To Develop knowledge in basic transistor logic.       2.       Y.1.0         Course Outcomes:       0.       To Develop knowledge in various programming platform like Altera, Xilinx.       Xilinx.         Course Outcomes:       0       Description       Outcomes       Course Outcomes:         On completion of the course, the student will be able to       Description       Outcomes       Course Outcomes:         CO1       Develop knowledge in programmable ASICS, programmable ASIC logic cells and programmbale ASIC I/O cells.       CO3       Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.       CO4       Develop knowledge in ASIC construction, floor planning, placement and routing.         UNIT-1       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC       12 Hours         UNIT-1       INTRODUCTION TO ASICS, PROGRAMMABLE ASIC I/O CELLS       12 Hours         UNIT-11       PROGRAMMABLE ASIC, PROGRAMMABLE ASIC I/O CELLS       12 Hours         UNIT-11       PROGRAMMABLE ASIC, PROGRAMMABLE ASIC I/O CELLS       12 Hours         Anti fuse –				-	-	Ŭ				
Course         Syllabus Revision         V.1.0           Category         Syllabus Revision         V.1.0           Pre- requisite         Course Objectives:         V.1.0           The course should enable the students -         1.         To Develop knowledge in basic transistor logic.           2.         To Develop knowledge in various programming platform like Altera, Xilinx.         Number State St		ASIC DESIGN	3	1	0	3	40	60	100	
Category       Pre- requisite         Pre- requisite       Course Objectives:         The course should enable the students - <ol> <li>To Develop knowledge in basic transistor logic.</li> <li>To Develop knowledge in various programming platform like Altera, Xilinx.</li> </ol> Course Outcomes:       Develop knowledge in various programming platform like Altera, Xilinx.         Course Outcomes:       Develop knowledge in Introduction TO ASICS, CMOS Logic and ASIC Library Design.         CO2       Develop knowledge in programmable ASICS, programmable ASIC logic cells and programmable ASIC I/O cells.         CO3       Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.         CO4       Develop knowledge in ASIC construction, floor planning, placement and routing.         UNIT-1       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN         Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.         UNIT-11       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC I/O CELLS       12 Hours         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.       12 Hours         UNIT-111       PROGRAMMABLE ASIC DESIGN S			-		-					
Pre- requisite       Course Objectives:         The course should enable the students -       1. To Develop knowledge in basic transistor logic.         2. To Develop knowledge in various programming platform like Altera, Xilinx.         Course Outcomes:       Develop knowledge in various programming platform like Altera, Xilinx.         Course Outcomes:       Description         Outcomes       Develop knowledge in Introduction TO ASICS, CMOS Logic and ASIC Library Design.         CO2       Develop knowledge in programmable ASICS, programmable ASIC logic cells and programmbale ASIC I/O cells.         CO3       Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.         CO4       Develop knowledge in ASIC construction, floor planning, placement and routing.         UNIT-I       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN         Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.         UNIT-II       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC I/O CELLS       12 Hours         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.       12 Hours         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASI	Course		Syllabus Revision					V.1.0		
requisite         Course Objectives:         The course should enable the students -         1.       To Develop knowledge in basic transistor logic.         2.       To Develop knowledge in various programming platform like Altera, Xilinx.         Course Outcomes:         On completion of the course, the student will be able to         Course Outcomes:         Outcomes       Description         C01       Develop knowledge in Introduction TO ASICS, CMOS Logic and ASIC Library Design.         C02       Develop knowledge in programmable ASIC, programmable ASIC logic cells and programmbale ASIC I/O cells.         C03       Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.         C04       Develop knowledge in logic synthesis, simulation and testing.         C05       Develop knowledge in ASIC construction, floor planning, placement and routing.         UNIT-11       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC Library architecture.         UNIT-11       INTRODUCTION TO ASICS, PROGRAMMABLE ASIC I/O cell.S         12 Hours       IJBRARY DESIGN         12 Hours       ILBRARY DESIGN         Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical e	<u> </u>									
Course Objectives:         The course should enable the students -         1.       To Develop knowledge in basic transistor logic.         2.       To Develop knowledge in various programming platform like Altera, Xilinx.         Course Outcomes:         On completion of the course, the student will be able to         Course Outcomes:         O1       Develop knowledge in Introduction TO ASICS, CMOS Logic and ASIC Library Design.         C02       Develop knowledge in programmable ASICS, programmable ASIC logic cells and programmbale ASIC I/O cells.         C03       Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.         C04       Develop knowledge in logic synthesis, simulation and testing.         C05       Develop knowledge in ASIC construction, floor planning, placement and routing.         UNIT-1       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC Library Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.         UNIT-11       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC I/O CELLS       12 Hours         LIGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS       12 Hours         LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS       12 Hours         LOGIC CELLS AND PROGRAMMBALE										
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On completion of the course, the student will be able to           Course         Description           Outcomes         Develop knowledge in Introduction TO ASICS, CMOS Logic and ASIC Library Design.           CO2         Develop knowledge in programmable ASICS, programmable ASIC logic cells and programmbale ASIC I/O cells.           CO3         Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.           CO4         Develop knowledge in logic synthesis, simulation and testing.           CO5         Develop knowledge in ASIC construction, floor planning, placement and routing.           UNIT-I         INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN         12 Hours           Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.           UNIT-II         PROGRAMMABLE ASICS, PROGRAMMABLE ASIC I/O CELLS         12 Hours           UNIT-III         PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC I/O Decklas         12 Hours           UNIT-III         PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY         12 Hours		<ul> <li>should enable the students -</li> <li>1. To Develop knowledge in basic transis</li> <li>2. To Develop knowledge in various prog</li> </ul>		•		orm	like	Altera	l,	
Course Outcomes         Description           CO1         Develop knowledge in Introduction TO ASICS, CMOS Logic and ASIC Library Design.           CO2         Develop knowledge in programmable ASICS, programmable ASIC logic cells and programmbale ASIC I/O cells.           CO3         Develop knowledge in programmable ASIC interconnect, programmable asic design software and low level design entry.           CO4         Develop knowledge in logic synthesis, simulation and testing.           CO5         Develop knowledge in ASIC construction, floor planning, placement and routing.           UNIT-I         INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN         12 Hours           Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.           UNIT-II         PROGRAMMABLE ASICS, PROGRAMMABLE ASIC I/O CELLS         12 Hours           Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.         12 Hours           UNIT-III         PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY         12 Hours										
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CO5       Develop knowledge in ASIC construction, floor planning, placement and routing.         UNIT-I       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN       12 Hours         Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.       12 Hours         UNIT-II       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS       12 Hours         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.       12 Hours         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY       12 Hours         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000       12 Hours						, I	e			
UNIT-I       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC       12 Hours         LIBRARY DESIGN       Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational       Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.       12 Hours         UNIT-II       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS       12 Hours         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.       12 Hours         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY       12 Hours	CO4	Develop knowledge in logic synthesis, simulat	tion	and	testing	<u>ş</u> .				
LIBRARY DESIGN         Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.         UNIT-II       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000	CO5	Develop knowledge in ASIC construction, flo	or p	lanni	ng, pl	acen	nent	and ro	uting.	
Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.         UNIT-II       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000	UNIT-I		GIC	ANI	) ASI	C		12 H	lours	
Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.         UNIT-II       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS       12 Hours         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.       12 Hours         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY       12 Hours         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000       1000 – Altera MAX 9000	Types of A	ASICs – Design Flow – CMOS transistors, CM	ЛОS	des	ign ru	ules	- Co	mbina	ational	
UNIT-II       PROGRAMMABLE ASICS, PROGRAMMABLE ASIC       12 Hours         LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS       12 Hours         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel       ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY       12 Hours         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000       12 Hours	Logic Cel	ll - Sequential logic cell - Data path logic	cel	1 – '	Transi	istor	s as	Resis	tors –	
LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS         Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel         ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock         and power inputs – Xilinx I/O blocks.         UNIT-III         PROGRAMMABLE ASIC INTERCONNECT,         PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW         LEVEL DESIGN ENTRY         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000	Transistor	Parasitic Capacitance – Logical effort – Library	y cel	l des	ign –	Libr	ary a	rchite	cture.	
ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and output s – Clock and power inputs – Xilinx I/O blocks.           UNIT-III         PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY         12 Hours           Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000         12 Hours	UNIT-II					LLS	5	12 H	lours	
and power inputs – Xilinx I/O blocks.         UNIT-III       PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY       12 Hours         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000	Anti fuse	- static RAM – EPROM and EEPROM techno	logy	/ – P	REP 1	benc	h ma	ırks –	Actel	
PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW         LEVEL DESIGN ENTRY       LEVEL DESIGN ENTRY         Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000			& A	C in	puts a	ind o	outpu	t s —	Clock	
	UNIT-III	PROGRAMMABLE ASIC DESIGN SOFT		-	AND	LO	W	12 H	lours	
Altera FLEX – Design systems – Logic Synthesis – Half Gate ASIC – Schematic entry of 58	Altera FLI	EX – Design systems – Logic Synthesis – Half	Gate	ASI	C - S	chen	natis	entry	ōf <b>58</b>	



Low leve	l design language – PLA tools – EDIF – CFI design representation.						
UNIT-IV	LOGIC SYNTHESIS, SIMULATION AND TESTING	12 Hours					
Verilog and	l logic synthesis – VHDL and logic synthesis - Types of simulation – Bo	oundary					
scan test –	Fault simulation – Automatic test pattern generation.						
UNIT-V	ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT	12 Hours					
	AND ROUTING						
System pa	artition – FPGA partitioning – partitioning methods – physical design flo	w – global					
routing –	detailed routing - specific DRC. floor planning - placement - al routing	g – circuit					
extraction	I.						
	Total Hours	60 Hours					
Text Book	(s)						
1.	M.J.S. SMITH, "Application – Specific Integrated Circuits" Add Longman Inc., 1997.	dison-Wesley					
2.		ndrew Brown, "VLSI Circuits and Systems in Silicon", Mc Graw Hill, 1991.					
3.	S.D.Brown, R.J.Francis, J.Rox, Z.G.Uranesic, "Field Programmable Gate Arrays" – Kluever Academic Publishers, 1992.						
	– Kluever Academic Publishers, 1992.						
4.	Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Processing", McGraw Hill, 1994.	Information					
4. 5.	Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and						



Γ		1	r —		n	n		1	
Course Code		L	Т	Р	С	IA	EA	ТМ	
Course									
Name	EMBEDDED LINUX	3	1	0	3	40	60	100	
Course Category		Syllabus Revision					V.	V.1.0	
Pre- requisite		•							
Course Ob	jectives:								
The course	should enable the students - 1. To Develop knowledge of usage of LT	NUX	( in )	Embec	dded	Syst	ems.		
Course Ou On complet	tcomes: ion of the course, the student will be able to								
Course	Description	1							
Outcomes	Let a let								
CO1	Understand how fundamentals of operating systems is used for embedded application.							edded	
CO2	Understand how linux fundamentals is used a	s an	OS	for em	bed	ded a	pplica	tion.	
CO3	Understand how embedded linux is used as an OS for embedded application.								
CO4	Understand how board support package and embedded storage is used as an Offor embedded application.						n OS		
CO5	Understand the how embedded drivers and application porting is used as an OS								
	for embedded application.	phe	unor	i porti		5 450	a us u		
UNIT-I	FUNDAMENTALS OF OPERATING SYS	TEN	ЛS				12H	ours	
Overview	of operating systems - Process and thread	s –	Pro	cesses	an	d Pr	ogram	ns –	
Programme	r view of processes - OS View of processes	5 - 7	Thre	ads -	Sch	eduli	ng –	Non	
preemptive	and preemptive scheduling - Real Time Sched	uling	g – P	rocess	s Syr	nchro	nizati	on –	
Semaphores	s - Message Passing - Mailboxes - Deadlocks	– Sy	nchi	onizat	tion	and s	chedu	ling	
in multipro	cessor Operating Systems.								
UNIT-II	LINUX FUNDAMENTALS						12H	ours	
Introduction	n to Linux - Basic Linux commands and conce	epts	- Lo	ogging	in -	Shel	1 s -B	asic	
text editing	- Advanced shells and shell scripting - Linux	File	Syst	em –L	linux	k Pro	gramn	ning	
- Processes calls.	and threads in Linux - Inter process communic	catio	n – 1	Devi c	es –	Linu	ıx Sys	stem	
UNIT-III	INTRODUCTION TO EMBEDDED LINU	X					12H	ours	
Embedded	Linux – Introduction – Advantages- En	nbed	ded	Linu	x I	Distri	bution	is -	
	e - Linux kernel architecture - User snace - lin								

Embedded Linux – Introduction – Advantages- Embedded Linux Distributions -Architecture - Linux kernel architecture - User space – linux startup sequence - GNU cross platform Tool chain.



UNIT-IV	BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE	12Hours				
Inclusion c	f BSP in kernel build procedure - The boot loader Interface - Memo	ry Map –				
Interrupt N	Aanagement – PCI Subsystem – Timers – UART – Power Mana	gement –				
Embedded	Storage - Flash Map - Memory Technology Device (MTD) - MTD Ar	chitecture				
- MTD Dri	ver for NOR Flash – The Flash Mapping drivers – MTD Block and cha	racter dev				
ices – mtd	utils package – Embedded File Systems – Optimizing storage space -	- Turning				
kernel men		Ũ				
UNIT-V	EMBEDDED DRIVERS AND APPLICATION PORTING	12Hours				
Linux seria	l driver – Ethernet driver – I2C subsystem – USB gadgets – Watchdo	og timer –				
	dules – Application porting roadmap - Programming with threads –	-				
	ting Layer – Kernel API Driver - Case studies - RT Linux – uClinux.	1 0				
	Total Hours	60Hours				
Text Book	(\$)					
1.	Dhananjay M. Dhamdhere, 'Operating Systems A concept based Approach',					
	Tata Mcgraw-Hill Publishing Company Ltd.					
2.	Matthias Kalle Dalheimer, Matt Welsh, 'Running Linux', O'Reilly P	ublications				
	2005.					
3.	Mark Mitchell, Jeffrey Oldham and Alex Samuel 'Advance	ced Linux				
4	Programming' New Riders Publications.	D .				
4.	P. Ragavan , Amol Lad , Sriram Neelakandan, 'Embedded Linux Syst	em Design				
5	and Development', Auerbach Publications, 2006.					
5.	Karim Yaghmour, 'Building Embedded Linux Systems', O'Reilly P 2003.	uoncations				
	2005.					



Course Code		L	Т	Р	С	IA	EA	TM
Course Name	VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	3	1	0	3	40	60	100
Course Category		S	yllal	ous R	evisi	on	V	/.1.0
Pre-								
requisite								
Course Obje								
The course sh	nould enable the students -							
	1. To have a knowledge in CMOS Design.							
	2. To Develop knowledge in PLD Devi							
	3. To have in floor plan design in VLSI	•						
Course Outc	omes:							
	on of the course, the student will be able to							
Course	Descript	ion						
Outcomes								
CO1	Develop knowledge and the understanding the CMOS design.	abo	ut th	e vari	ous	aspec	ets inv	olved in
CO2	Develop knowledge and the understanding	aboı	ıt th	e vari	ous	aspec	ets inv	olved in
	the programable logic devices.							
CO3	Develop knowledge and the understanding the ASIC construction, floor planning, placed					aspec	ets inv	olved in
CO4	Develop knowledge and the understanding					aspec	ets inv	olved in
	the analog VLSI design.							
CO5	Develop knowledge and the understanding	aboı	it th	e vari	ous	aspec	ets inv	olved in
	the logic synthesis and simulation.					-		
UNIT-I	CMOS DESIGN						<b>12</b> H	lours
circuits-Clo	f digital VLSI design Methodologies- Logic ocked CMOS-dynamic CMOS circuits, Bi-CM fabrications – Trends in IC technology.							e
UNIT-II	PROGRAMABLE LOGIC DEVICES						<b>12</b> H	ours
Programming	g Techniques-Anti fuse-SRAM-EPROM	ar	d	EEPR	OM	te	chnol	ogy –
6	nable Devices Architecture- Function blocks							05
•	l Runner - XC-4000,XC5200, SPARTAN	-					,	
10KStratix.		,					_ ,0	
UNIT-III	ASIC CONSTRUCTION, FLOOR PLAN AND ROUTING	NIN	G,P	LAC	EMI	ENT	12 H	lours



System partition – FPGA partitioning – Partitioning methods- floor planning – placement physical design flow – global routing – detailed routing – special routing- circuit extraction – DRC

		10.11
UNIT-IV	ANALOG VLSI DESIGN	12 Hours
Introduction	to analog VLSI- Design of CMOS 2stage-3 stage Op-Amp –High Spec	ed and High
frequency op	-amps-Super MOS-Analog primitive cells-realization of neural networ	rks.
UNIT-V	LOGIC SYNTHESIS AND SIMULATION	12 Hours
Overview of	digital design with Verilog HDL, hierarchical modelling concepts,	modules and
port definition	ons, gate level modelling, data flow modelling, behavioural mode	elling, task &
functions, Ve	erilog and logic synthesis-simulation-Design examples, Ripple carry	Adders, Carry
Look ahead a	dders, Multiplier, ALU, Shift Registers, Multiplexer, Comparator, Tes	st Bench.
	Total Hours	60 Hours
Text Book(s	)	
1.	M.J.S Smith, "Application Specific integrated circuits", Add	lition Wesley
	Longman Inc.1997.	
2.	Kamran Eshraghian, Douglas A.pucknell and Sholeh Eshraghian,"	Essentials of
	VLSI circuits and system", Prentice Hall India,2005.	
3.	Wayne Wolf, "Modern VLSI design " Prentice Hall India,200	6. ACC.NO:
	B134477	
4.	Mohamed Ismail, Terri Fiez, "Analog VLSI Signal and	information
	processing", McGraw Hill International Editions, 1994.	
4. 5.		





Course Name       PRINCIPLES OF ROBOTICS       3       1       0       3       40       60       100         Course Category       Syllabus Revision       V.1.0         Pre- requisite       Syllabus Revision       V.1.0         Course Objectives:       0       3       40       60       100         Course Objectives:       1. To have basic knowledge about robotics.       2. To Develop knowledge in image processing and Vision.         Course Outcomes:       0       Description       Outcomes         Outcomes       Description       Outcomes       CO2       Understanding the various aspects of robotics and how image and vision systems are processed.       Zelonation & velocities.       Zelonation & velocities.         CO3       Understanding the various aspects of fobot control system.       ZO4       Understanding the various aspects of image processing & vision systems.         UNIT-1       INTRODUCTION AND TERMINOLOGIES       12Hours         Definition-Classification-History-       Robots components-Degrees of freedom-Robot joints coordinates-       Reference frames-workspace-Robot languages-actuators-sensors-Position, velocity and acceleration sensors-Torque sensors-tactile and touch sensors proximity and range sensors-social issues.         UNIT-11       KINEMATICS       12Hours         Mcchanism-matrix representation-homogenous transformation-DH representation- Inverse k	Course Code		L	Т	Р	С	IA	EA	ТМ
Category       Prc- requisite         Prc- requisite       Course Objectives:         The course should enable the students - <ul> <li>1. To have basic knowledge about robotics.</li> <li>2. To Develop knowledge in image processing and Vision.</li> </ul> Course Outcomes:       Description         Outcomes       Description         Outcomes       Outestanding the various aspects of robotics and how image and vision systems are processed.         CO2       Understanding the various aspects of differential motion & velocities.         CO3       Understanding the various aspects of fobot control system.         CO5       Understanding the various aspects of finage processing & vision systems.         UNIT-1       INTRODUCTION AND TERMINOLOGIES       12Hours         Definition-Classification-History-       Robots components-Degrees of freedom-Robot joints coordinates-         Reference       frames-workspace-Robot languages-actuators-sensors-Position, velocity and acceleration sensors-Torque sensors-tactile and touch sensors proximity and range sensors-social issues.         UNIT-11       KINEMATICS       12Hours         Mechanism-matrix representation-homogenous transformation-DH representation- Inverse kinematics-solution and programming-degeneracy and dexterity.       12Hours         UNIT-11       DIFFERENTIAL MOTION & VELOCITIES       12Hours         Sensor characteristics-       Hydraulic	Course Name	PRINCIPLES OF ROBOTICS	3	1	0	3	40	60	100
Pre- requisite       Image: Should enable the students -         1. To have basic knowledge about robotics.       2. To Develop knowledge in image processing and Vision.         Course Outcomes:         On completion of the course, the student will be able to         Course       Description         Outcomes       Description         C01       Understanding the various aspects of robotics and how image and vision systems are processed.         C02       Understanding the various aspects of differential motion & velocities.         C03       Understanding the various aspects of robot control system.         C04       Understanding the various aspects of image processing & vision systems.         C05       Understanding the various aspects of image processing & vision systems.         C06       Understanding the various aspects of image processing & vision systems.         C05       Understanding the various aspects of image processing & vision systems.         UNIT-11       INTRODUCTION AND TERMINOLOGIES       12Hours         Definition-Classification-History- Robots components-Degrees of freedom-Robot joints coordinates- Reference frames-workspace-Robot languages-actuators-sensors-Position, velocity and acceleration sensors-Torque sensors-tactile and touch sensors proximity and range sensors-social issues.       12Hours         UNIT-11       KINEMATICS       12Hours         Mechanism-matrix representation-homogenous tra	Course Category		Syllabus Revision						1.0
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decentralised PID control- non-linear decoupling control. UNIT-V IMAGE PROCESSING & VISION SYSTEMS 12Hours	Sensor cha	racteristics- Hydraulic, Pneumatic and elect	tric	actua	ators-1	traie	ctorv	plan	ning
UNIT-V IMAGE PROCESSING & VISION SYSTEMS 12Hours		-	-		~~			1	0
	UNIT-V	IMAGE PROCESSING & VISION SYSTI	EMS					12H	ours
TWO AND TOTAL OUR UNIONAL IMAGENENDATIAL AND DECODED AV DOMAIN TEDIENEMATION-DOINE AND					repre	sent	ation-		



edges-convolution masks-Processing techniques - thresholding - noise reduction edge detection-segmentation-Image analysis and object recognition.

	Total Hours 60Hours
Text Book(	s)
1.	Saeed B. Niku ,"Introduction to Robotics ", Pearson Education, 2002 ACC.NO: B66274.
2.	Fu, Gonzalez and Lee Mcgrahill ,"Robotics ", international ACC.NO: B135132.
3.	R.D. Klafter, TA Chmielewski and Michael Negin, "Robotic Engineering, An Integrated approach", Prentice Hall of India, 2003. ACC.NO: B19966.



		L	Т	Р	С	IA	EA	ТМ		
Code	ADDI ICATIONS OF MEMS									
Course Name	APPLICATIONS OF MEMS TECHNOLOGY	3	1	0	3	40	60	100		
Course		Syllabus Revision V.1.0								
Category										
Pre-										
requisite										
Course Ob										
The course	should enable the students -			<b>1</b> · .						
	1. To Develop knowledge in the basic of M				on.					
	2. To Develop knowledge about sensors in	ME	MS.							
Course Ou	tcomes: ion of the course, the student will be able to									
Course	Descriptio	n								
Outcomes	Descriptio	/11								
CO1	Develop knowledge in basic of MEMS: Mic	ro-F	abri	cation	Mat	terial	s and	Electro		
001	Mechanical Concepts.			,						
CO2	Develop knowledge in basic of electrostatic s	enso	rs a	nd actu	iatio	n.				
CO3	Develop knowledge in basic of Thermal Sens									
CO4	Develop knowledge in basic of Piezoelectric					ion.				
CO5	Develop knowledge in Sensors used for the ap									
UNIT-I	MEMS: MICRO-FABRICATION, MATE	RIA	LS A	AND			<b>12</b> H	lours		
	ELECTRO MECHANICAL CONCEPTS									
	funiana fabrication Siliaan and other mot	erial	bas	ed fat	orica	tion	proces	ses -		
Overview o	of micro faorication – Silicon and other mat	oriur					-	3505		
	of micro fabrication – Silicon and other mat Conductivity of semiconductors-Crystal plane		d oi	rientati	on-s	tress	and			
Concepts:	Conductivity of semiconductors-Crystal plane	s an						strain-		
Concepts: ( flexural bea	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri	s an						strain-		
Concepts: ( flexural bea quality fact	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or.	s an nsic	stre	ss- res			equenc	strain- cy and		
Concepts: ( flexural bea quality factor UNIT-II	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or. ELECTROSTATIC SENSORS AND ACTI	s an nsic UAT	stre	ss- res	sonai	nt fre	equenc	strain- cy and lours		
Concepts: ( flexural bea quality fact UNIT-II Principle, n	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or.	s an nsic UAT	stre	ss- res	sonai	nt fre	equenc	strain- cy and lours		
Concepts: ( flexural bea quality fact UNIT-II Principle, m and actuato	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or. ELECTROSTATIC SENSORS AND ACT naterial, design and fabrication of parallel plat	s an nsic UAT e ca	stre	ss- res	sonai	nt fre	equence 12 H catic se	strain- cy and lours ensors		
Concepts: ( flexural bea quality fact UNIT-II Principle, n and actuato	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or. ELECTROSTATIC SENSORS AND ACTU naterial, design and fabrication of parallel plat rs-Applications. THERMAL SENSING AND ACTUATION	s an nsic UAT e ca	stre	ss- res		nt fre	equence 12 H catic se 12 H	strain- cy and lours ensors		
Concepts: ( flexural bea quality fact UNIT-II Principle, m and actuato UNIT-III Principle, m	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or. ELECTROSTATIC SENSORS AND ACTI naterial, design and fabrication of parallel plat rs-Applications.	s an nsic UAT e ca	stre	ss- res		nt fre	equence 12 H catic se 12 H	strain- ey and lours ensors		
Concepts: ( flexural bea quality fact UNIT-II Principle, n and actuato UNIT-III Principle, 1 thermal resi	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or. ELECTROSTATIC SENSORS AND ACTUN naterial, design and fabrication of parallel plat rs-Applications. THERMAL SENSING AND ACTUATION naterial, design and fabrication of thermal istor sensors-Applications.	s an nsic UAT e ca I coup	stre	ss- res		nt fre	equence 12 H catic se 12 H rph se	strain- cy and lours ensors lours ensors,		
Concepts: ( flexural bea quality fact UNIT-II Principle, n and actuato UNIT-III Principle, 1 thermal resi	Conductivity of semiconductors-Crystal plane am bending analysis-torsional deflections-Intri or. ELECTROSTATIC SENSORS AND ACTUN naterial, design and fabrication of parallel plat rs-Applications. THERMAL SENSING AND ACTUATION naterial, design and fabrication of thermal	s an nsic UAT e ca Coup	stre	ss- res	elec	oimoi	equence 12 H catic se 12 H rph se 12 H	strain- cy and lours ensors msors, lours		



UNIT-V	CASE STUDIES	12 Hours
Piezoresist	ive sensors, Magnetic actuation, Microfluidics applications, Medical a	applications,
Optical MI	EMS.	
		·
	Total Hours	60 Hours
<b>Text Book</b>	(s)	
1.	Chang Liu, "Foundations of MEMS", Pearson International Edi	tion, 2006.
	ACC.NO: B127890.	
2.	Marc Madou, "Fundamentals of microfabrication", CRC Press, 199	7. ACC.NO:
	B130141	
3.	Boston, "Micromachined Transducers Sourcebook", WCB McGraw I	Hill, 1998.
4.	M.H.Bao "Micromechanical transducers : Pressure sensors, acceler	rometers and
	gyroscopes", Elsevier, New york, 2000.	



Course		L	Т	Р	С	IA	EA	ТМ
Code		L	1	1	U	IA	LA	I IVI
Course	DIGITAL IMAGE PROCESSING	2	1	0	2	40	(0)	100
Name		3	1	0	3	40	60	100
Course		S	vllał	nis Re	visi	on	V	1.0
Category		Syllabus Revision V.1						1.0
Pre-								
requisite								
Course Ob	iectives:							
	should enable the students -							
	1. To have a knowledge in basic of Ima	ge Pi	roce	ssing.				
	2. To have a knowledge in various analysis of image.							
	3. To Develop knowledge in application			-	proc	essin	g is	
	used.			0	L		0	
Course Out	tcomes:							
	ion of the course, the student will be able to							
Course	Description	1						
Outcomes	- ···· <b>p</b> ····							
CO1	Develop knowledge and understanding the ba	asic (	conc	epts o	f im	age 1	proces	sing,
	image analysis and the application fundament							0,
CO2	Develop knowledge and understanding the bas	sic co	once	pts im	age	enhai	nceme	ent.
CO3	Develop knowledge and understanding the b	asic	con	cepts	imag	ge seg	gment	ation
	and feature analysis.							
<b>CO4</b>	Develop knowledge and understanding the	bas	sic (	concep	ts n	nulti	resol	ution
	analysis and compressions.							
CO5	Develop knowledge and understanding the ba	asic	conc	cepts a	ppli	catio	n of i	mage
	processing.							
							4.4.11	
UNIT-I	FUNDAMENTALS OF IMAGE PROCESS						12H	
	n – Steps in image processing systems – Im							
Quantization	n – Pixel relationships – Color fundamentals	and	moc	lels, F	ile f	òrma	ts, In	nage
operations -	- Arithmetic, Geometric and Morphological.							
UNIT-II	IMAGE ENHANCEMENT						12H	ours
Spatial Dor	nain: Gray level Transformations – Histogram	m pi	roce	ssing -	- Sp	oatial	filter	ring
smoothing a	and sharpening. Frequency Domain: Filtering ir	ı free	quer	ncy do	mair	n – D	FT F	FT,
-	othing and sharpening filters – Homomorphic F		-	5			,	ý
	o r r r r	•						
UNIT-III	IMAGE SEGMENTATION AND FEATUR	RE A	NΔ				12H	ours
	f Discontinuities – Edge operators – Edge lin					w D		
			-			-		
	g – Region based segmentation – Morph	10108	lical	wate	ersne	eas -	- M0	uon
Segmentatio	on, Feature Analysis and Extraction.							



UNIT-IV	MULTI RESOLUTION ANALYSIS AND COMPRESSIONS	<b>12Hours</b>
Multi Rese	olution Analysis: Image Pyramids - Multi resolution expansion -	Wavelet
Transforms	s, Image compression: Fundamentals – Models – Elements of Informatio	n Theory
– Error free	e compression – Lossy Compression – Compression Standards.	
	ADDI ICATION OF IMACE DROCESSING	1311
UNIT-V	APPLICATION OF IMAGE PROCESSING	12Hours
Image class	sification – Image recognition – Image understanding – Video motion an	alysis –
		5
Image fusio	on – Steganography – Digital compositing Mosaics – Colour Image Proc	5
Image fusio	on – Steganography – Digital compositing Mosaics – Colour Image Proc	5
Image fusio	on – Steganography – Digital compositing Mosaics – Colour Image Proc Total Hours	5
Image fusio	Total Hours	essing.
	Total Hours	essing. 60Hours
Text Book	(s)	essing. 60Hours
Text Book	Total Hours (s) Rafael C.Gonzalez and Richard E.Woods, "Digital Image Processin	60Hours
Text Book	Total Hours (s) Rafael C.Gonzalez and Richard E.Woods, "Digital Image Processin Edition, Pearson Education, 2003. ACC.NO: B134341.	60Hours
Text Book	Total Hours (s) Rafael C.Gonzalez and Richard E.Woods, "Digital Image Processin Edition, Pearson Education, 2003. ACC.NO: B134341. Milan Sonka, Valclav Halavac and Roger Boyle, "Image Processing, J	essing. 60Hours ng", 2nd Analysis



Course Code		L	Т	Р	С	IA	EA	ТМ		
Course Name	EMBEDDED ANALOG INTERFACING	3	1	0	3	40	60	100		
Course Category	Syllabus Revision V.1.0									
Pre- requisite										
Course Ob	jectives:									
	should enable the students -									
	1. To have a basic knowledge in measurement system design.									
	2. To have a knowledge in Analog to Digit	al Co	onve	rters.						
	3. To have a knowledge in Sensors used in	inte	rfaci	ng.						
Course Ou	taamas									
	tion of the course, the student will be able to									
Course	Description	n								
Outcomes	- ···· F ····									
CO1	Develop knowledge and understanding measu	reme	ent s	ystem	desi	gn.				
CO2	Develop knowledge and understanding in anal	log-t	o-di	gital c	onve	rters.				
CO3	Develop knowledge and understanding in sense	sors	& pe	ripher	als.					
CO4	Develop knowledge and understanding in outp	out c	ontr	ol met	hods					
CO5	Develop knowledge and understanding in mic	roco	ntro	ller int	erfa	cing.				
UNIT-I	MEASUREMENT SYSTEM DESIGN						12H	ours		
Characteris	tics of Instrumentation – Measurement accuracy	V —	Mea	surem	ent	sta	ndard	s –		
	ange – Calibration – Bandwidth – Digital interf									
UNIT-II	ANALOG-TO-DIGITAL CONVERTERS						12H	01116		
	ADCs - ADC Comparison - Sample and Ho	ld -	ΔΓ		neg	- Fla				
• •	Approximation ADC - Dual-Slope (Integration			-	-					
					-					
Embedded (	ssor Interfacing - Clocked Interfaces - Ser	141	mel	Taues	- 1	integr	aicu	ADC		
Enibedded	Controllers.									
UNIT-III	SENSORS & PERIPHERALS						12H	ours		
Temperatur	e Sensors - Optical Sensors - CCDs - Magnet	tic S	ensc	ors-]	Moti	on/A	cceler	ation		
Sensors -	Strain Gauges - Solenoids – Heaters – Coo	olers	- ]	LEDs	– I	DACs	– D	igital		
	ters - Analog Switches - Stepper Motors - DC N							-		
	<b>C</b> 11									



UNIT-IV	OUTPUT CONTROL METHODS	12Hours				
Measuring	Period versus Frequency - Voltage-to-Frequency Converters - O	pen-Loop				
Control - N	Negative Feedback and Control - Microprocessor-Based Systems- On-O	ff Control				
– Proporti	onal Control - Proportional, Integral, Derivative Control - Motor	Control -				
Predictive	Predictive Control - Measuring and Analyzing Control Loops.					
UNIT-V	MICROCONTROLLER INTERFACING	12Hours				
Standard I	nterfaces - IEEE 1451.2 - 4-20 ma Current Loop - Field bus - Micro	controller				
Supply and	d Reference - Resistor Networks - Multiple Input Control -AC Control	- Voltage				
Monitors	and Supervisory Circuits - Driving Bipolar Transistors/ MOSFET-	Reading				
Negative V	Voltages – PWM based control.					
	Total Hours	60Hours				
Text Book	s(s)					
1.	Stuart R. Ball, Analog Interfacing to Embedded Microprocessor	Systems,				
	Newnes, 2nd Edition ,2003.					
2.	John G. Webster, Handbook of measurement, Instrumentation, & ser	nsors, John				
ļ	Wiley & Sons Inc, New York-1998.					
3.	Dogan Ibrahim, Microcontroller-Based Temperature Monitoring	and				
	Control, Newnes, 2nd Edition ,2002.					



Course Code		L	Т	Р	С	IA	EA	ТМ	
Course Name	EMBEDDED AUTOMOTIVE NETWORKING WITH CAN	3	1	0	3	40	60	100	
Course Category		Syllabus Revision V.1.							
Pre-		I					I		
requisite									
Course Ob The course	should enable the students -								
	1. To Develop knowledge in basic of data communication.								
	2. To have a knowledge in Layers of CAN	Net	work	ζ.					
Course Ou	tcomes:								
_	ion of the course, the student will be able to								
Course	Description	1							
Outcomes CO1	Develop knowledge and understand the basic	ofd	ata a		niaa	tion			
CO1 CO2	Develop knowledge and understand the basic								
C02	Develop knowledge and understand the basic								
CO4	Develop knowledge and understand the basic								
CO5	Develop knowledge and understand the basic								
UNIT-I	DATA COMMUNICATION BASICS						12H	ours	
	munication basics - Network communication p	roto	col -	- Med	ium	acces			
	checking & control – Requirements & app								
	stics of CAN.						5		
							-		
UNIT-II	CAN DATA LINK LAYER						12H		
	link layer – Principles of bus arbitration – Fi				Err	or de	etectio	n &	
error hand	lling – Extended frame format – Time triggered	mul	tiple	xing.					
UNIT-III	CAN PHYSICAL LAYER						12H	ours	
	gnaling – Transmission media – Network to	polo	gv -	- Bus	med	lium			
-	ver standards.	[	05						
UNIT-IV	CAN PROTOCOL CONTROLLERS						12H	ours	
CAN proto	col controllers – Functions of a CAN control	ler –	Me	ssage	filte	ring	– Mes	ssage	
handling - S	Standalone CAN controllers – Integrated CAN c	contr	oller	s - C	AN 1	transe	ceiver	S.	
UNIT-V	CAN HIGHER LAYER PROTOCOLS						12H	ours	
	lication layer – Protocol architecture – CAN m	iessa	ige s	pecifi	catio	n – 7			
	ge identifiers – Network management – Lay		-	-					
		,		<u> </u>		2	/	2	



protocols - CAN open – Device Net – SAEJ1939 – Time triggered CAN.						
	Total Hours 60Hours					
Text Book	(\$)					
1.	Konrad Etschberger, Controller Area Network, IXXAT Automation GmbH, 2001.					
2.	Wolfhard Lawrenz, CAN System Engineering: From Theory to Practical Applications, Springer, 1997.					
3.	Glaf P.Feiffer, Andrew Ayre and Christian Keyold "Embedded Networking with CAN and CAN open". Embedded System Academy 2005.					
4.	Francoise Simonot-Lion, Handbook of Automotive Embedded Systems ,CRC Press,2007.					
5.	http://www.can-cia.org/can/.					
6.	http://www.semiconductors.bosch.de/en/20/can/3-literature.asp.					



Course		_		_					
Code		L	Т	Р	С	IA	EA	TM	
Course	EMBEDDED SYSTEM DESIGN USING				Ì				
Name	ARM PROCESSOR								
		3	1	0	3	40	60	100	
Course		S	vllal	bus Re	l evisi	on	v	V.1.0	
Category		~	<i>J</i> 1144	54514	0 1 1 5 1	011			
Pre-									
requisite									
Course Obj	ectives:								
The course s	should enable the students -								
	1. To have a knowledge about ARM funda	men	tals.						
	2. To have a knowledge of writing codes.								
<b>Course Out</b>	comes:								
On completi	on of the course, the student will be able to								
Course	Description						Hig	ghest	
Outcomes							Blo	Bloom's	
								onomy	
CO1	Develop knowledge in the fundamentals of p							1.	
CO2	Develop knowledge in the fundamentals of A					dame	ntals.		
CO3	Develop knowledge in the fundamentals of c								
CO4	Develop knowledge in the fundamentals of o								
CO5	Develop knowledge in the fundamentals of A	ARM	pro	cessor	and	und	erstan	d how to	
	write the assembly code in ARM.								
UNIT-I	PRINCIPLES OF EMBEDDED SYSTEM						12 H	lours	
Introductio			ion	desid	τn	consi			
	nts - Overview of Embedded system Arch			-	-				
-	5				•				
-	- Product specifications - hardware/softw		-		-				
-	ation – hardware software integration -	-			-		-		
	ation Protocols: UART – Inter Integrated Circ					-			
. ,	ntroller Area Network (CAN).Wireless commu	unica	ation	Proto	ocols	: Z1g	bee P	rotocols	
– Bl ue too	th Protocols - IrDA.								
UNIT-II	ARM PROCESSOR FUNDAMENTALS						12 H	lours	
ARM core	Introduction - Registers - Current Program St	atus	Reg	ister –	Pip	eline	– Exc	eption	
<ul> <li>Interrupt</li> </ul>	s - Vector Table - Core Extension - Archit	ectu	re R	evisio	ns –	ARI	M Pro	cessor	
-	ARM Instruction Set - Thumb Instruction set								
	erworking – Stack Instruction – Software Inter-			-			-		
	<u> </u>	··· T· •							
UNIT-III	CACHES AND MMU						1 <b>7</b> P	lours	
		٨٠٠٠	hita	ture	Ca	aha			
	ry Hierarchy and Cache Memory - Cache	AIC	mee	Jule	- Ca	iche	rone	y - CO	



Processor and Caches – Flushing and Cleaning Cache Memory – Cache Lockdown – Caches and Software Performance. MMU: Moving from an MPU to an MMU – Virtual Memory – Details of ARM MMU – The Caches and Write Buffer – Co Processor and MMU configuration.

UNIT-IV	OPTIMIZED PRIMITIVES	12 Hours					
Double Pre	Double Precision Integer Multiplication - Integer Normalization and count Leading Zeros -						
Division –	Square Roots - Transcendental Functions : Log,, exp, sin, cos - End	ian Reversal					
and Bit Op	erations - Saturated and Rounded Arithmetic - Random Number Gene	ration.					
UNIT-V	WRITING AND OPTIMIZING ARM ASSEMBLY CODE	12 Hours					
Writing Ass	embly Code - Profiling and Cycle Counting - Instruct ion Schedulin	ng – Register					
Allocation -	Allocation - Conditional Execution - Looping Constructs - Bit Manipulation - Efficient						
Switches – H	Switches – Handling Unaligned Data.						
	Total Hours	60 Hours					
Toxt Book							

Text Book(s	S)
1.	Andrew N.Sloss, Dominic Symes, Chris Wright, "ARM System Developer's
	Guide", Morgan Kaufmann Series in Computer Architecture and Design, 2004.
2.	Tammy Noergaard, "Embedded Systems Architecture", Newnes, 2005. ACC.NO:
	B127886
3.	David Seal, "ARM Architecture Reference Manual", 2005.
4.	Steve Furbe, "ARM System-on-Chip Architecture", Addison-Wesley Professional,
	2nd Edition, 2000, ACC.NO: B129645.



Code       DISTRIBUTED EMBEDDED       3       1       0       3       40       60       100         Course       COMPUTING       3       1       0       3       40       60       100         Course       Syllabus Revision       V.1.0       V.1.0       100       100         Course Objectives:       In the students -       1.       1.       10.0       3       40       60       100         Course Objectives:       In the a knowledge of the Hardware Infrastructure.       2.       To have a knowledge of the using of JAVA in Distributed Embedded Computing.       4.       To have a knowledge of embedded computing architectures.         Course Outcomes:       On completion of the course, the student will be able to       Course Outcomes.       CO1       Develop knowledge and understand the concept of andware infrastructure.       CO2         CO1       Develop knowledge and understand the concept of distributed computing using java.       Develop knowledge and understand the concept of embedded agent.       CO3       Develop knowledge and understand the concept of embedded agent.       CO4       Develop knowledge and understand the concept of embedded agent.       CO5       Develop knowledge and understand the concept of embedded agent.       CO5       Develop knowledge and understand the concept of embedded agent.       CO4       Develop knowledge and understand the concept of embedded	Course		L	Т	Р	С	IA	EA	ТМ
Name       COMPUTING       3       1       0       3       40       60       100         Course Category       Syllabus Revision       V.1.0         Pre- requisite       Syllabus Revision       V.1.0         Course Objectives:       V.1.0       V.1.0         The course should enable the students -       1. To have a knowledge of the Hardware Infrastructure.       V.1.0         2. To have a knowledge of the using of JAVA in Distributed Embedded Computing.       To have a knowledge of embedded computing architectures.         4. To have a knowledge of embedded computing architectures.       Course Outcomes:       Description         Outcomes       Description       Description       Image: CO1       Develop knowledge and understand the concept of distributed computing using java.         CO3       Develop knowledge and understand the concept of embedded agent.       CO3       Develop knowledge and understand the concept of embedded agent.         CO4       Develop knowledge and understand the concept of embedded computing using java.       Image: Provemation Provematication Provematicatena Networks Provemates Provematication Prov	Code		L	1	1	Ľ	IA	LA	1 111
Nume         COMPORTING           Course         Syllabus Revision         V.1.0           Category         Pre- requisite         Syllabus Revision         V.1.0           Pre- requisite         Syllabus Revision         V.1.0           Course Objectives:         In course should enable the students -         In course a knowledge of the using of JAVA in Distributed Embedded Computing.         A. To have a knowledge of embedded computing architectures.           Course Outcomes:         On completion of the course, the student will be able to         Course         Course           Course         Develop knowledge and understand the concept of hardware infrastructure.         CO2         Develop knowledge and understand the concept of distributed computing using java.           CO4         Develop knowledge and understand the concept of embedded agent.         CO5         Develop knowledge and understand the concept of embedded computing using java.           CO5         Develop knowledge and understand the concept of embedded agent.         CO5         Develop knowledge and understand the concept of embedded computing using java.           CO4         Develop knowledge and understand the concept of embedded agent.         CO5         Develop knowledge and understand the concept of embedded agent.         CO5           UNIT-1         THE HARDWARE INFRASTRUCTURE         12Hours         Broad Band Transmission facilities – Open Interconnection standards – Local Area Net			2	1	0	2	40	60	100
Category       Pre- requisite         Course Objectives:         The course should enable the students - <ul> <li>1. To have a knowledge of the Hardware Infrastructure.</li> <li>2. To have a knowledge of the using of JAVA in Distributed Embedded Computing.</li> <li>4. To have a knowledge of embedded computing architectures.</li> </ul> Course Outcomes:         On completion of the course, the student will be able to           Course Outcomes:         Description           Outcomes         Description           CO1         Develop knowledge and understand the concept of hardware infrastructure.           CO2         Develop knowledge and understand the concept of internet concepts.           CO3         Develop knowledge and understand the concept of embedded agent.           CO4         Develop knowledge and understand the concept of embedded agent.           CO5         Develop knowledge and understand the concept of embedded agent.           CO4         Develop knowledge and understand the concept of embedded agent.           CO5         Develop knowledge and understand the concept of embedded agent.           CO4         Develop knowledge and understand the concept of embedded agent.           CO5         Develop knowledge and understand the concept of embedded agent.           CO4         Develop knowledge and understand the concept of embedded computing architecture.	Name	COMPUTING	5	1	0	3	40	00	100
Pre- requisite       requisite         Course Objectives:       1. To have a knowledge of the Hardware Infrastructure.         2. To have a knowledge the concept of Internet.       3. To have a knowledge of the using of JAVA in Distributed Embedded Computing.         4. To have a knowledge of embedded computing architectures.       0. To have a knowledge of embedded computing architectures.         Course Outcomes:       0n completion of the course, the student will be able to         Course       Description         Outcomes       Develop knowledge and understand the concept of internet concepts.         CO1       Develop knowledge and understand the concept of distributed computing using java.         CO4       Develop knowledge and understand the concept of embedded agent.         CO5       Develop knowledge and understand the concept of embedded computing using java.         CO4       Develop knowledge and understand the concept of embedded computing architecture.         UNIT-I       THE HARDWARE INFRASTRUCTURE       12Hours         Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Network management – Network Security – Cluster computers.       12Hours         UNIT-II       INTERNET CONCEPTS       12Hours         Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.         UNIT-II	Course		S	yllat	ous Re	evisi	on	V.	1.0
requisite       Course Objectives:         The course should enable the students - <ol> <li>To have a knowledge of the Hardware Infrastructure.</li> <li>To have a knowledge of the using of JAVA in Distributed Embedded Computing.</li> <li>To have a knowledge of embedded computing architectures.</li> </ol> Course Outcomes:           On completion of the course, the student will be able to           Course           Outcomes           Outcomes           Outcomes           Outcomes           Outcomes         Description           Outcomes         Develop knowledge and understand the concept of hardware infrastructure.         CO2         Develop knowledge and understand the concept of distributed computing using java.         Develop knowledge and understand the concept of embedded agent.         CO5 <ld>Develop knowledge and understand the concept of embedded computing using achitecture.         I2Hours           UNIT-I         THE HARDWARE INFRASTRUCTURE         12Hours         I2Hours           Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Weide Area Networks – Network management – Network Security – Cluster computers.         I2Hours           UNIT-II         INTERNET CONCEPTS         12Hours           Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and X</ld>	Category								
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1. To have a knowledge of the Hardware Infrastructure.         2. To have a knowledge the concept of Internet.         3. To have a knowledge of the using of JAVA in Distributed Embedded Computing.         4. To have a knowledge of embedded computing architectures.         Course Outcomes:         On completion of the course, the student will be able to         Course       Description         Outcomes       Description         C01       Develop knowledge and understand the concept of hardware infrastructure.         C02       Develop knowledge and understand the concept of distributed computing using java.         C04       Develop knowledge and understand the concept of embedded agent.         C05       Develop knowledge and understand the concept of embedded computing using architecture.         UNIT-1       THE HARDWARE INFRASTRUCTURE       12Hours         Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.       UNIT-1I         UNIT-11       INTERNET CONCEPTS       12Hours         Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.         UNIT-11       DISTRIBUTED COMPUTING USING JAVA       12Hours         IO streaming – Object serialization – Networking – Threading – RM I – mu									
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3. To have a knowledge of the using of JAVA in Distributed Embedded Computing.       4. To have a knowledge of embedded computing architectures.         Course Outcomes:         On completion of the course, the student will be able to         Course       Description         Outcomes       Develop knowledge and understand the concept of hardware infrastructure.         CO2       Develop knowledge and understand the concept of distributed computing using java.         CO4       Develop knowledge and understand the concept of embedded agent.         CO5       Develop knowledge and understand the concept of embedded computing using java.         CO4       Develop knowledge and understand the concept of embedded agent.         CO5       Develop knowledge and understand the concept of embedded computing architecture.         UNIT-I       THE HARDWARE INFRASTRUCTURE       12Hours         Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Weide Area Networks – Network management – Network Security – Cluster computers.       UNIT-II         UNIT-II       INTERNET CONCEPTS       12Hours         Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.       UNIT-II         UNIT-II       DISTRIBUTED COMPUTING USING JAVA       12Hours         IO streaming – Object serialization – Networking – Threading		-							
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4. To have a knowledge of embedded computing architectures.         Course Outcomes:         On completion of the course, the student will be able to         Course       Description         Outcomes       Description         CO1       Develop knowledge and understand the concept of hardware infrastructure.         CO2       Develop knowledge and understand the concept of distributed computing using java.         CO4       Develop knowledge and understand the concept of embedded agent.         CO5       Develop knowledge and understand the concept of embedded agent.         CO5       Develop knowledge and understand the concept of embedded computing architecture.         UNIT-I       THE HARDWARE INFRASTRUCTURE       12Hours         Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.       UNIT-II         UNIT-II       INTERNET CONCEPTS       12Hours         Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.         UNIT-II       DISTRIBUTED COMPUTING USING JAVA       12Hours         IO streaming – Object serialization – Networking – Threading – RM I – multicasting – distributed databases – embedded agents – case studies.       12Hours         Introduction to the embedded agents – Embedded agent design									
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On completion of the course, the student will be able to           Course Outcomes         Description           CO1         Develop knowledge and understand the concept of hardware infrastructure.           CO2         Develop knowledge and understand the concept of internet concepts.           CO3         Develop knowledge and understand the concept of distributed computing using java.           CO4         Develop knowledge and understand the concept of embedded agent.           CO5         Develop knowledge and understand the concept of embedded computing architecture.           UNIT-I         THE HARDWARE INFRASTRUCTURE         12Hours           Broad Band         Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.         12Hours           Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.         12Hours           IO streaming – Object serialization – Networking – Threading – RM I – multicasting – distributed databases – embedded java concepts – case studies.         12Hours           Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks			-8						
Course Outcomes         Description           CO1         Develop knowledge and understand the concept of hardware infrastructure.           CO2         Develop knowledge and understand the concept of internet concepts.           CO3         Develop knowledge and understand the concept of distributed computing using java.           CO4         Develop knowledge and understand the concept of embedded agent.           CO5         Develop knowledge and understand the concept of embedded computing architecture.           UNIT-1         THE HARDWARE INFRASTRUCTURE         12Hours           Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.         12Hours           Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.         12Hours           IO streaming – Object serialization – Networking – Threading – RM I – multicasting – distributed databases – embedded java concepts – case studies.         12Hours           Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks	Course Ou	tcomes:							
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CO5       Develop knowledge and understand the concept of embedded computing architecture.         UNIT-I       THE HARDWARE INFRASTRUCTURE       12Hours         Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.       12Hours         UNIT-II       INTERNET CONCEPTS       12Hours         Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.       12Hours         IO streaming – Object serialization – Networking – Threading – RM I – multicasting – distributed databases – embedded java concepts – case studies.       12Hours         Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks       12Hours	CO4	5	pt of	emt	bedded	lage	ent.		
UNIT-I       THE HARDWARE INFRASTRUCTURE       12Hours         Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks       – Wide Area Networks – Network management – Network Security – Cluster computers.         UNIT-II       INTERNET CONCEPTS       12Hours         Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.       12Hours         UNIT-III       DISTRIBUTED COMPUTING USING JAVA       12Hours         IO streaming – Object serialization – Networking – Threading – RM I – multicasting – distributed databases – embedded java concepts – case studies.       12Hours         UNIT-IV       EMBEDDED AGENT       12Hours         Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks								comp	uting
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– Wide Area Networks – Network management – Network Security – Cluster computers.         UNIT-II       INTERNET CONCEPTS       12Hours         Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.       12Hours         UNIT-III       DISTRIBUTED COMPUTING USING JAVA       12Hours         IO streaming – Object serialization – Networking – Threading – RM I – multicasting – distributed databases – embedded java concepts – case studies.       12Hours         UNIT-IV       EMBEDDED AGENT       12Hours         Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks									
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Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.         UNIT-III       DISTRIBUTED COMPUTING USING JAVA       12Hours         IO streaming – Object serialization – Networking – Threading – RM I – multicasting – distributed databases – embedded java concepts – case studies.       12Hours         UNIT-IV       EMBEDDED AGENT       12Hours         Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks		1							
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UNIT-III       DISTRIBUTED COMPUTING USING JAVA       12Hours         IO streaming – Object serialization – Networking – Threading – RM I – multicasting –       distributed databases – embedded java concepts – case studies.         UNIT-IV       EMBEDDED AGENT       12Hours         Introduction to the embedded agents – Embedded agent design criteria – Behaviour based,       Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks	-		•						
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UNIT-IV         EMBEDDED AGENT         12Hours           Introduction to the embedded agents – Embedded agent design criteria – Behaviour based,         Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks				ing -	- RM	I –	mult	ticasti	ng –
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Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks								n	
Functionality based embedded agents - Agent co-ordination mechanisms and benchmarks	UNIT-IV								
			-						
embedded_agent Case study: Mobile robots			ion	mecł	nanisn	ns ar	nd be	enchm	arks
undeueu-agent. Case study. 19100115 100015.	embedded-a	agent. Case study: Mobile robots.							



UNIT-V	EMBEDDED COMPUTING ARCHITECTURE	12Hours
Synthesis of	f the information technologies of distributed embedded systems - anal	log/digital
co-design -	optimizing functional distribution in complex system design - valid	lation and
fast prototy	ping of multiprocessor system-on-chip – a new dynamic scheduling algo	orithm for
real-time m	ultiprocessor systems.	
	Total Hours	60Hours
Text Book(	s)	
1.	Dietel & Dietel, "JAVA how to program", Prentice Hall 1999.	ACC.NO:
	B112846	
2.	Sape Mullender, "Distributed Systems", Addison-Wesley, 1993.	
3.	George Coulouris and Jean Dollimore, "Distributed Systems - con c	epts and
	design", Addison – Wesley 1988.	
4.	"Architecture and Design of Distributed Embedded Systems", edited	•
	Kleinjohann C-lab, Universitat Paderborn, Germany, Kluwer	Academic
	Publishers, Boston, April 2001.	





Course		L	Т	Р	С	IA	EA	ТМ
Code Course	SMART METERS AND SMART GRID							
Name	COMMUNICATION OBJECTIVES	3	1	0	3	40	60	100
Course Category		S	V.1.0					
Pre-								
requisite								
Course Ob								
The course	should enable the students -							
	1. To teach the fundamentals of automated	mete	ers ar	d Grie	ds.			
	2. To teach on functional components of St	mart	mete	rs.				
	3. To discuss on need of smart grid for pov	ver sy	/sten	IS.				
	4. To teach the significance of microgrid and	nd its	need	ls.				
	5. To teach the communication and protoco				stem	l <b>.</b>		
	1		1	5				
Course Ou	tcomes:							
On comple	tion of the course, the student will be able to							
Course	Descript	ion						
Outcomes								
CO1	Understandable knowledge in the autom	nated	gri	d and	1 m	eters	func	lamental,
	significance of micro grid and the protocols	used	for	the co	mm	unica	tion a	s well as
	power system.							
CO2	Understandable knowledge in the smart meter							
CO3	Understandable knowledge in the smart grid a	nd ap	plica	ations.				
CO4	Understandable knowledge in the microgrids.							
CO5	Understandable knowledge in the information smart grid and meters.	on a	nd c	ommu	nıca	tion	techno	ology for
UNIT-I	INTRODUCTION						12 H	lours
	on to Smart grid and metering technology-	Sm	art e	nerav	ma	nagei		
	re-Functions of Smart Grid and smart meters, C					-		
	conventional and smart grid-meters, Concept of							
	0 1						•	u, lecent
developin	ents and International policies in Smart Grid. IF	C 01	830	protoc	of st	anuai	us.	
LINIT II							10 1	[
UNIT-II	SMART METERS		0		1 •			lours
	ering-Smart Meters types- hardware architectur						-	
	tion protocols- Real Time Prizing, Smart A							•
MEMS, Sn	hart Sensors- Smart actuators- Advanced meterin	ng int	frastr	ucture	e- sp	ectrui	n anal	yzer.
UNIT-III	SMART GRID AND APPLICATIONS						12 H	lours
Outage Ma	nagement System, Plug in Hybrid Electric V	Vehic	les,	Vehic	le to	o Gri	d, Ho	me and
e	utomation- Smart Substations, Substation Autor		-				,	
-	System(GIS), Intelligent Electronic Devices a							
	-Smart city- Wide Area Measurement Syste							-
Protection-	Smart enty while Area wiedsurement Syste	, II, I	11450		Sure		ge 55 o	



Quality and	EMC in Smart Grid, Power Quality issues of Grid connected Renewable Energy					
	ower Quality Conditioners for Smart Grid, Web based Power Quality monitoring and					
<b>Cours</b> Qual	Ity Audit.					
Code						
UNIT-IV	MICROGRIDS 12 Hours					
	microgrid, need and applications of microgrid, formation of microgrid, Issues of					
	tion, protection and control of microgrid. Plastic and Organic solar cells, Thin film					
	Variable speed wind generators, fuel cells, microturbines, Captive power plants,					
Integration	of renewable energy sources.					
UNIT-V	INFORMATION AND COMMUNICATION TECHNOLOGY12 HoursFOR SMART GRID AND METERS12 Hours					
Home Area	a Networks for smart grid - IEEE 802.15.4 - ITU G.hn-IEEE 802.11, Field Area					
Networks ·	-power-line communications- IEEE P1901 / Home Plug, RF mesh, Wide-area					
Networks for	or Smart Grid- Fiber Optics, Wi-MAX, sensor networks, Information Management in					
Smart Grid	-SCADA, CIM. Networking Issues in Smart Grid -Wireless Mesh Network- Cloud					
Computing	-Security and Privacy in Smart Grid and smart meters -Broadband over Power line.					
	Total Hours 60 Hours					
Text Book(						
1.	Ali Keyhani, Mohammad N. Marwali, Min Dai "Integration of Green and Renewable Energy in Electric Power Systems", Wiley.					
2.	Stuart Borlase, "Smart Grid: infrastructure, technology and Solutions", 2012 CRC.					
3.	Janaka Ekanayake, Nick Jenkins, Kithsiri Liyanage, Jianzhong Wu, Akihiko Yokoyama, "Smart Grid: Technology and Applications", Wiley.					
4.	Jean Claude Sabonnadière, Nouredine Hadjsaïd, "Smart Grids", Wiley Blackwell.					
5.	Peter S. Fox Penner, "Smart Power: Climate Changes, the Smart Grid, and the Future of Electric Utilities", Island Press; 1 edition 8 Jun 2010.					
6.	S. Chowdhury, S. P. Chowdhury, P. Crossley, "Microgrids and Active Distribution Networks." Institution of Engineering and Technology, 30 Jun 2009.					
7.	Stuart Borlase, "Smart Grids (Power Engineering)", CRC Press.					
<b>Reference</b>						
1	Andres Carvallo, John Cooper, "The Advanced Smart Grid: Edge Power Driving Sustainability: 1", Artech House Publishers July 2011.					
2.	James Northcote, Green, Robert G. Wilson "Control and Automation of Electric Power Distribution Systems (Power Engineering)", CRC Press.					
3	Mladen Kezunovic, Mark G. Adamiak, Alexander P. Apostolov, Jeffrey George Gilbert "Substation Automation (Power Electronics and Power Systems)", Springer.					
4.	R. C. Dugan, Mark F. McGranghan, Surya Santoso, H. Wayne Beaty, "Electrical Power System Quality", 2nd Edition, McGraw Hill Publication.					
5.	Yang Xiao, "Communication and Networking in Smart Grids", CRC Press.					



Course Name	SOFT COMPUTING TECHNIQUES	3	1	0	3	40	60	100
Course Category		Syllabus Revision						V.1.0
Pre-								
requisite								
Course Ob	-							
The course	should enable the students -							
	1. To review the fundamentals of ANN and	d fuz	zy s	et the	ory.			
	2. To make the students understand the use	e of	AN	V for 1	node	eling	and co	ontrol of
	non-linear system and to get familiarized	d wit	th th	e ANI	N an	d FL	C tool	box.
	3. To make the students to understand the u		-				-	
	4. To familiarize the students on various h	ybri	d co	ntrol s	scher	nes, l	P.S.O	and get
	familiarized with the ANFIS tool box.							
Course Ou								
-	ion of the course, the student will be able to							
Course	Descripti	on						
Outcomes CO1	Develop knowledge and understand the	vori	0110	0.000.00	ata	of or	ft or	monuting
COI	techniques. overview of artificial neural netw			-				mputing
CO2	Develop knowledge and understand the var							orks for
	modelling and control.		F					
CO3	Develop knowledge and understand the variou	is as	pect	s of f	uzzy	logic	for n	odelling
	and control.							
CO4	Develop knowledge and understand the variou		•	-		-		
CO5	Develop knowledge and understand the variou	is as	pect	s of h	ybrie	d con	trol sc	hemes.
IINIT I	OVEDVIEW OF ADTIFICIAL NEUDAL					-D	10 1	<b>.</b>
UNIT-I	OVERVIEW OF ARTIFICIAL NEURAL	NEI	wc	ЭКК (		N)	12 H	lours
	& FUZZY LOGIC			<b>.</b>		6	<u> </u>	0: 1
	fundamentals - Biological neuron, Artificial							-
2	eptron – Limitations – Multi Layer Perceptron -		1	10		U		
-	neory – Fuzzy sets – Operation on Fuzzy sets -				-		-	-
	intersection, complement (yager and sugen							
1 0	composition, decomposition, cylindrical e	xten	sion	, fuz	zy 1	relation	on –	Fuzzy
membership	o functions.							
	Γ							
UNIT-II	NEURAL NETWORKS FOR MODELLIN							lours
_	f non linear systems using ANN- NARX,NNS							-
-	al architecture - Model validation- Control of			-		-		
	t neuro control schemes- Adaptive neuro contro	oller	– Ca	ase sti	ıdy -	Fam	iliariz	ation of
Neural Netw	vork Control Tool Box.							



UNIT-III	FUZZY LOGIC FOR MODELLING AND CONTROL	12 Hours
Modeling o	of non linear systems using fuzzy models (Mamdani and Sugeno) -	FSK model -
Fuzzy Log	ic controller - Fuzzification - Knowledge base - Decision mak	king logic –
Defuzzifica	tion-Adaptive fuzzy systems - Case study - Familiarization of Fuzzy	/ Logic Tool
Box.		
	CENETIC AL CODITIIM	12 11
UNIT-IV	GENETIC ALGORITHM	12 Hours
	ept of Genetic algorithm and detail algorithmic steps, adjustment of fre	-
	typical control problems using genetic algorithm. Concept on some	other search
techniques	like Tabu search, Ant-colony search and Particle Swarm Optimization.	
	1	
UNIT-V	HYBRID CONTROL SCHEMES	12 Hours
Fuzzificatio	on and rule base using ANN-Neurofuzzy systems - ANFIS - Op	timization of
membershi	p function and rule base using Genetic Algorithm and Particle Swarm G	Optimization -
Case study-	-Introduction to Support Vector Regression – Familiarization of ANFIS	Tool Box.
		(0 H
	Total Hours	60 Hours
Text Book		• • • • • • • • • • • • • • • • • • •
1.	Laurene V.Fausett, "Fundamentals of Neural Networks, Architecture and Applications", Pearson Education, 2008.	e, Algorithms,
2.	Timothy J.Ross, "Fuzzy Logic with Engineering Applications", Wiley	/.
3.	George J.Klir and Bo Yuan, "Fuzzy Sets and Fuzzy Logic:	
1	Applications", Prentice Hall, First Edition, 1995. ACC.NO: B132844	
4.	David E.Goldberg, "Genetic Algorithms in Search, Optimization, Learning", Pearson Education, 2009.	and Machine
5.	W.T.Miller, R.S.Sutton and P.J.Webrose, "Neural Networks for C	Control" MIT
5.	Press, 1996.	
6.	C.Cortes and V.Vapnik, "Support-Vector Networks, Machine Learnin	g", 1995.