SRI CHANDRASEKHARENDRA SARASWATHI VISWA MAHAVIDYALAYA

[SCSVMV]

(Deemed to be University u/s 3 of the UGC Act, 1956)

Accredited with "A" Grade by NAAC

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Analog and Digital ElectronicsLab Manual

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Prepared by

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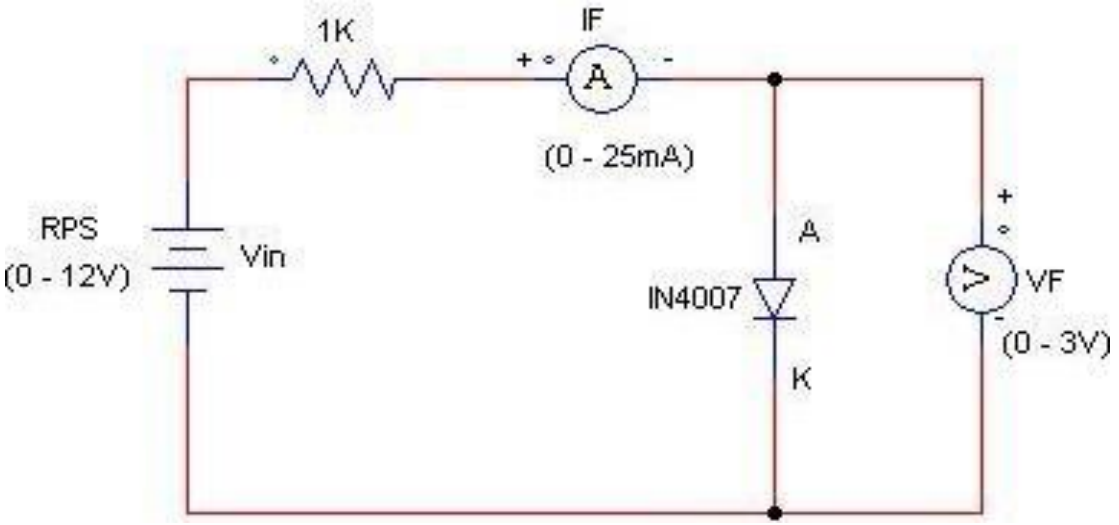
INSTRUCTIONS TO STUDENTS WORKING IN ELECTRICAL AND ELECTRONICS LABORATORIES

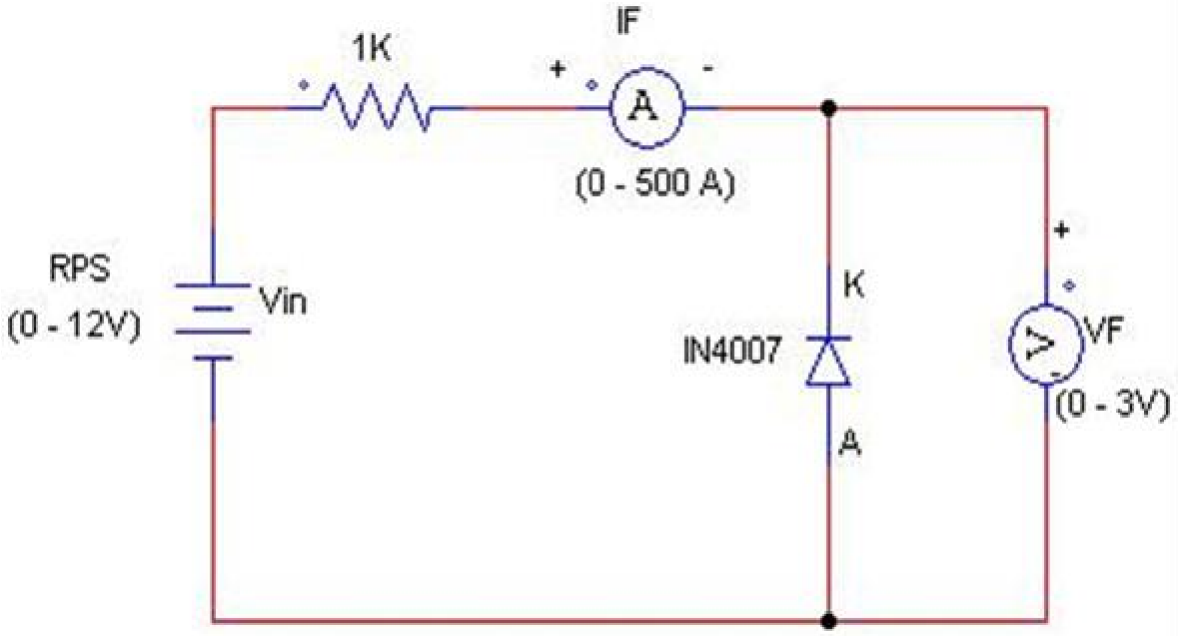
1. Every student should come with right fitting dress & wear shoes with rubber soles.
2. Every student should avoid wearing metal ornaments like ring, bangles, bracelets, chains etc.
3. The circuit diagrams should be approved by the Teaching faculty in the laboratory.
4. The approved indent slip should be given in the store and receive the apparatus box.
5. These apparatus must be brought from the stores and kept on the worktable in a neat manner, such a way that the connections are made conveniently.
6. Make the connections as per the diagram approved.
7. Get the connections be checked by the Lab Instructor in charge in the laboratory.
8. The Lab Instructor will arrange to give the supply to the worktable.
9. After ascertaining, the supply is given to the worktable, and students can proceed to conduct the experiment as per the instruction issued.
10. If there is any difficulty experienced in the conduct of the experiment immediately call the Lab Instructor and get over the difficulty.
11. After finishing the experiment, switch off the supply, show the observations to the Lab Instructor, and get approved.
12. Request the Lab Instructor to make arrangements to switch off the supply to the worktable.
13. After ascertaining that the supply is switched off, disconnect and return the apparatus box to the store.
14. Complete experiment should be recorded in the laboratory record notebook and shown to the Teaching faculty in the next class.
15. If there is any damage to any material during transit or conduct of the experiment, all the students in that particular group/batch are responsible.
16. Every student should take utmost care not to touch any live points, while they work in the laboratory.
17. Every student should keep his/her laboratory record with his/her safely till the concerned practical examination is over

CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS



EX.NO: **DATE:**

CHARACTERISTICS OF SEMI CONDUCTOR DIODE

AIM: -

To draw the V-I characteristics of a p-n junction diode and to find the forward resistance RF and cut- in voltage.

APPARATUS REQUIRED: -

S.No	NAME	RANGE	QUANTITY
1	PN Junction diode	IN4007	1
2	Resistor	1 K	1
3	Ammeter	0-50 mA, 0-500 A	Each 1
4	Voltmeter	0-30V, 0-3V	Each 1
5	RPS	0-30V	1
6	Bread board	-	1

THEORY: -

When a P and N type semi-conductor are formed together a P-N junction is created. There are two types of biasing. When a P-type semiconductor is connected to positive terminal of the battery and N-type Semiconductor is to the negative terminal, the junction barrier vanishes and we get forward current. But When connections are interchanged the junction barrier increases very much and there is no current flow. But a small value of current, due to the minority carriers, known as reverse saturation current, is presentthere.

TABULATION:

FORWARD BIAS:

SL.NO	V_{IN}(V)	V_F(V)	I_F (A)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			

REVERSE BIAS:

SL.NO	V_{IN}(V)	V_R(V)	I_R (A)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			

PROCEDURE:

FORWARD CHARACTERISTICS:

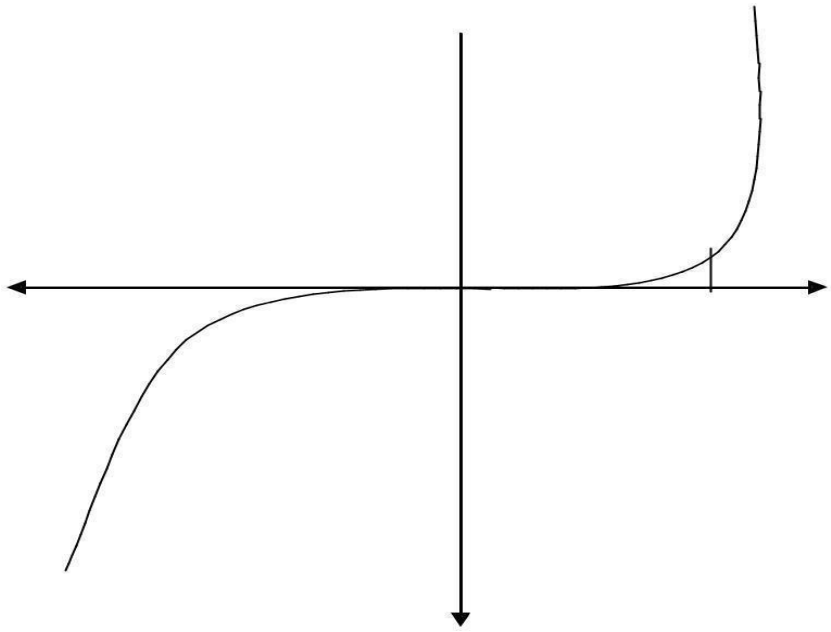
1. The connections are made as per the circuit diagram.
2. Input supply voltage is varied.
3. The corresponding forward voltage and current are noted.
4. The readings are tabulated and the graph is plotted between the voltage on x-axis and current on y-axis.
5. From the graph the forward resistance RF = Vf/ If cut-in voltage are calculated.

REVERSE BIAS CHARACTERISTICS:

1. The terminals are reversed and the above steps are repeated. To find Forward Resistance

$$R_F = V_f / I_f$$

MODEL GRAPH:



MODEL CALCULATION:

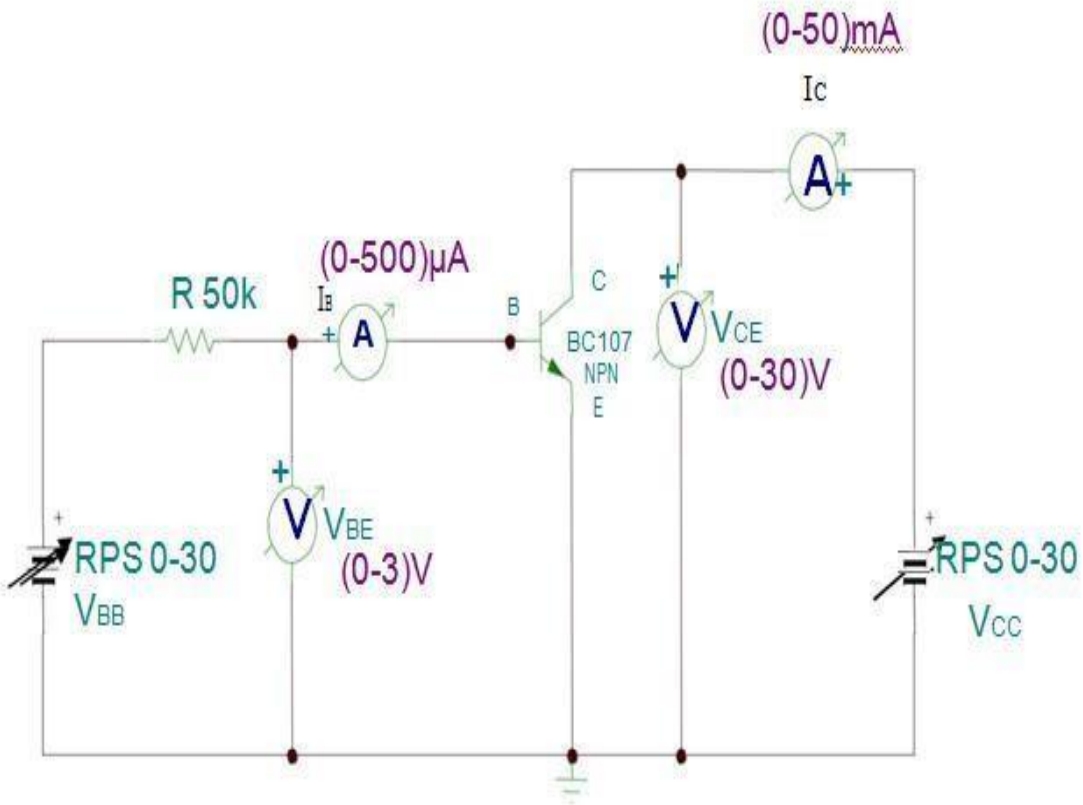
RESULT: -

Thus, the forward and reverse characteristics of a P-N junction diode were plotted andfollowing observations were made.

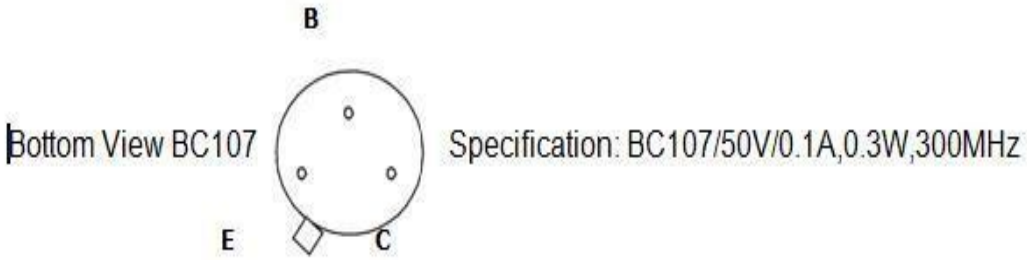
Forward resistance :

Cut-in voltage :

Circuit Diagram:



PIN DIAGRAM:



EX.NO : **DATE :**

CHARACTERISTICS OF BJT IN CE MODE

AIM:

To draw the input and output characteristics of the Bipolar Junction transistor in Common Emitter Mode.

APPARATUS REQUIRED:

S.No	NAME	RANGE	QUANTITY
1	Transistor	BC107	1
2	Resistor	50 K	1
3	Voltmeter	0-50V	1
4	Ammeter	0-50 mA, 0-500 A	Each 1
5	Bread board	-	1

THEORY: -

It is nothing but two junction diodes connected back to back. There is three region named as Emitter, Base and Collector. The base is lightly doped , collector moderately and emitter heavily. The emitter region is made larger to dissipate heat energy. The function of emitter region is to inject charge carriers to the base, which, in turn pass to the collector. The collector collects the charge carriers from the base or emitter.

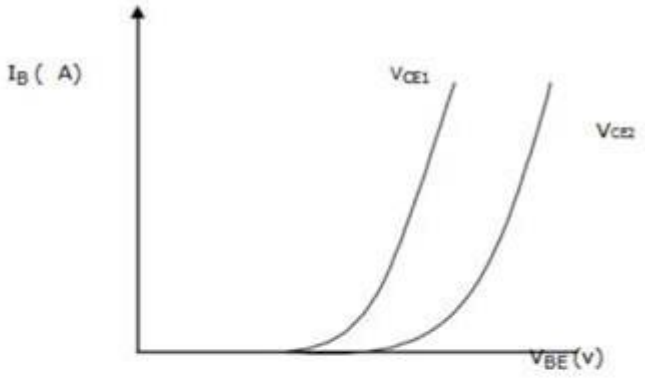
PROCEDURE:

INPUT CHARACTERISTICS:

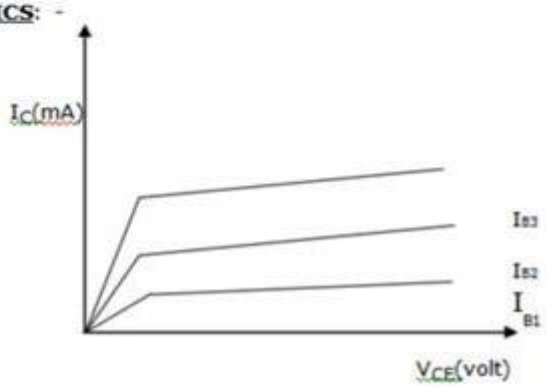
1) Connections are made as per the circuit diagram.
2) The output voltage VCE is kept constant.
3) By varying the input voltage VBE , the corresponding input currents IB are noted down
4) A graph is plotted between VBE and IB.
5) The inverse slope of the curve gives forward input resistance

MODEL GRAPH:

INPUT CHARACTERISTICS:-



OUTPUT CHARECTERSTICS: -



OUTPUT CHARACTERISTICS :

1. The connections are made as per the circuit diagram.
2. The input current I_B is kept constant.
3. By varying the output voltage V_{CE} , the corresponding output current I_C is noted down.
4. A graph is plotted between V_{CE} and I_C .
5. The inverse slope of the curve gives forward output resistance

FORMULA:

$\mathbf{R_i = \Delta V_{BE} / \Delta I_B}$

$\mathbf{R_0 = \Delta V_{CE} / \Delta I_C}$

MODEL CALCULATION:

TABULATION :

INPUT CHARACTERISTICS:

V_{CE}:_____V

SL.NO	V_{BB}(V)	V_{BE}(V)	I_B (A)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			

OUTPUT CHARACTERISTICS:

I_B:_____A

SL.NO	V_{CC}(V)	V_{CE}(V)	I_C (A)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			

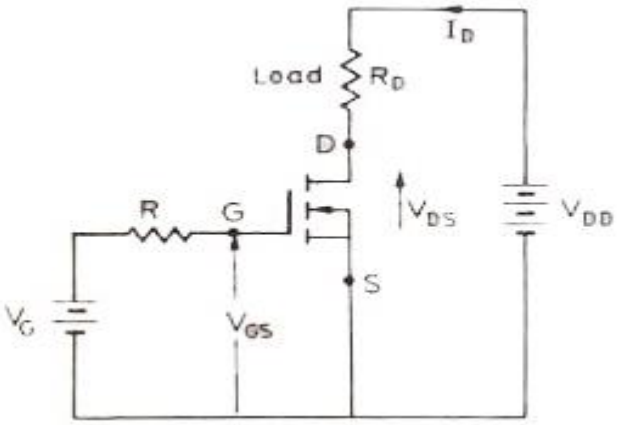
RESULT: -

The input and output characteristics of the transistor in CE mode are drawn and the input and output resistances are calculated.

Input resistance=

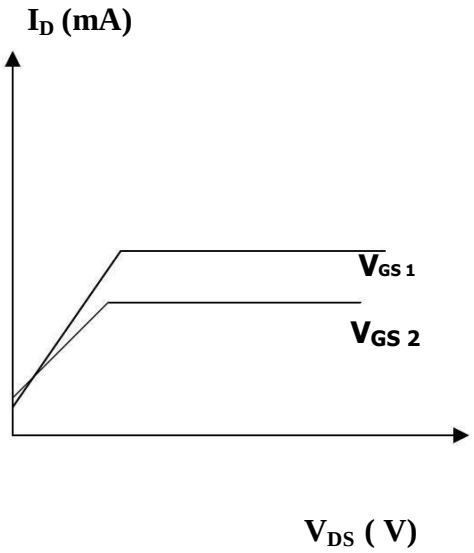
Output resistance =

CIRCUIT DIAGRAM:

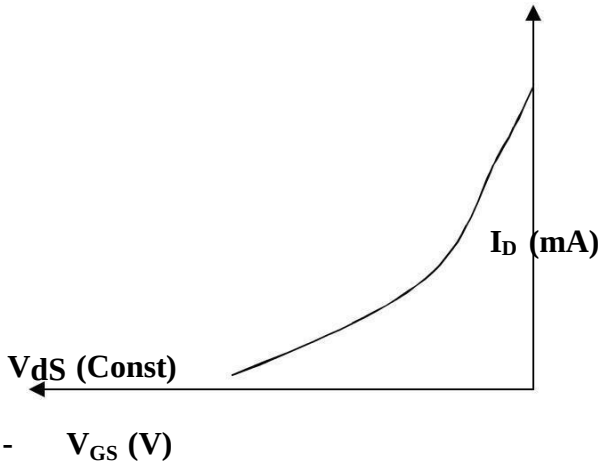


MODEL GRAPH:-

DRAIN CHARACTERISTICS:



TRANSFER CHARACTERISTICS:-



EX.NO : **DATE :**

DRAIN AND TRANSFER CHARACTERISTICS OF MOSFET

AIM

To study and plot the drain and transfer characteristics of MOSFET

APPARATUS REQUIRED:

S.No	NAME	RANGE	QUANTITY
1	MOSFET	IR150	1
2	Ammeter	0-25 mA	1
3	Voltmeter	0-30V	1
4	Resistor	1K	1
5	RPS	0-30V	2
6	Bread board	-	1

THEORY:

MOSFET is an abbreviation for metal oxide semiconductor filed transistor. Like JFET, it has a source (S), drain(D) and gate(G). However unlike JFET, the gate of MOSFET is insulated from channel. Because of this, MOSFET is sometimes known as IGFET(insulated gate FET). Basically MOSFET are of two types

1) depletion type MOSFET and 2) enhancement type MOSFET.

Enhancement MOSFET has no depletion mode and only operates in enhancement mode. It differs in construction from depletion type MOSFET in the sense that it has no physical channel. The min gate- source voltage (VGS), which produces inversion layer, called as threshold voltage.

TABULATION:

Drain Characteristics:

SL.NO	V_S (v)	V_{GS} =	
		V_{DS} (V)	I_D (mA)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			
20.			
21.			
22.			
23.			
24.			
25.			

Transfer Characteristics:

Sl.NO	V_S (v)	V_{GS} =	
		V_{DS} (V)	I_D (mA)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
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24.			
25.			

DRAIN CHARACTERISTICS FOR ENHANCEMENT MOSFET: -

When $V_{GS} < V_S$ the no drain current flows. However in actual practice, and extremely small value of drain current does flow through MOSFET. This current flow is generally due to presence of thermally generated electron in P type substrate when value of V_{GS} is kept above (V_{GS}) significant drain current flow.

TRANSFER CHARACTERISTICS OF MOSFET: -

When $V_{GS}=0$ there is no drain current, however if V_{GS} is increased rapidly. The relation gives the drain current at any instant along the curve.

$I_D=k\ [(V_{GS}-V_{GS})]$

PROCEDURE: -

DETERMINATION OF DRAIN CHARACTERISTICS:

1. Voltage V_{GS} is kept at some fixed level.
2. The Drain to Source voltage V_{DS} is varied and the corresponding drain current Id is noted. TheGraph was plotted between V_{DS} on the x-axis and I_d on y-axis.
3. The drain resistance (r_d) was determined as $r_d = V_{DS}/ I_d$

DETERMINATION OF TRANSFER CHARACTERISTICS:

1. The V_{DS} is kept at some particular value.
2. The Source voltage V_{GS} is varied at some particular level and the corresponding drain current I_d was noted.
3. A graph was plotted between V_{GS} and I_D.
4. The transfer conductance value was determined by $g_m = I_d/ V_{GS}$.

DETERMINATION OF AMPLIFICATION FACTOR:

Amplification factor $\mu = g_m * r_d$

RESULT: -

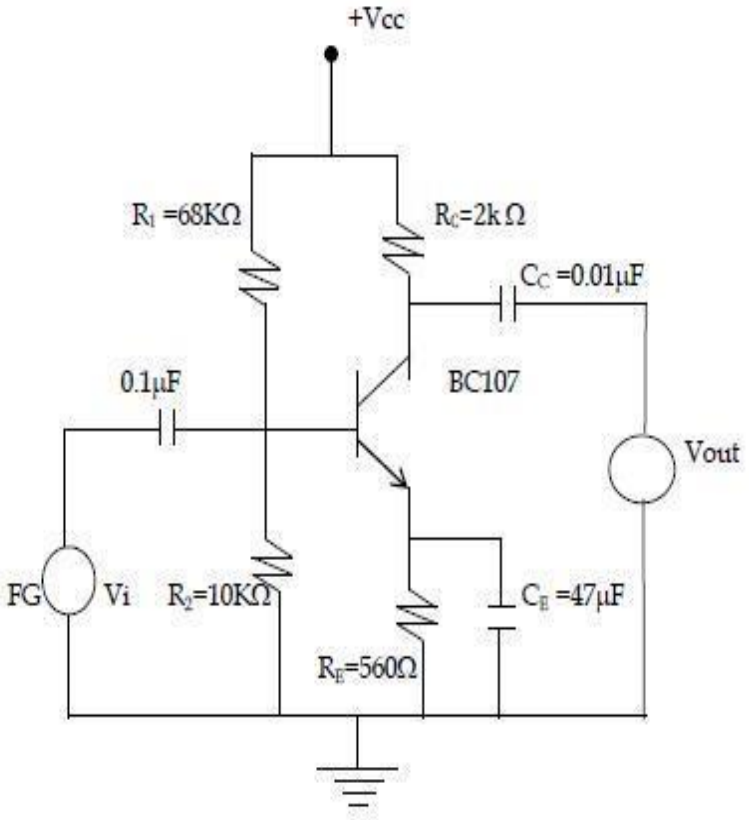
Thus the Drain and transfer characteristics of the given MOSFET were studied and the following values were determined.

a) Drain resistance (r_d) =

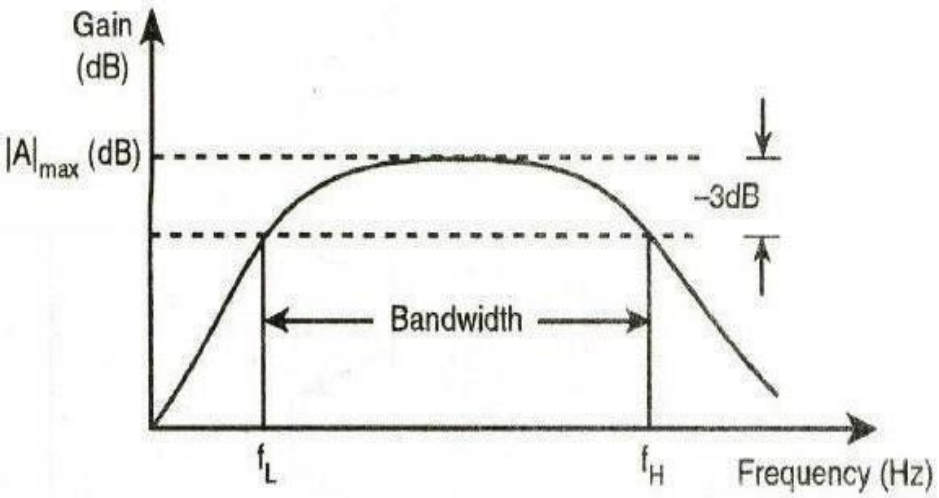
b) Trans-Conductance (g_m) =

c) Amplification factor (μ) =

CIRCUIT DIAGRAM



MODEL GRAPH:



EX.NO : **DATE :**

COMMON EMITTER AMPLIFIER

AIM:-

To study the frequency response of common emitter amplifier.

APPARATUS REQUIRED

SL. No	APPARATUS	RANGE	QTY
1.	Transistor (BC -107)		
2.	Regulated Power Supply		
3.	Resistor		
4.	Capacitor		
5.	Function Generator		
6.	C.R.O		
7.	Bread Board & connecting wires		

THEORY:

An amplifier is an electronic circuit that is capable of increasing the level of the signal applied at its input.The semiconductor devices used for the purpose of amplification are transistors. When a transistor is biased in active region it acts like an amplifier. We apply an ac voltage between the base and emitter terminals to producecorresponding collector current.

An amplified output signal is obtained when this fluctuating collector current flows through a collector resistor Rc.

The capacitor across the collector resistor Rc will act as a bypass capacitor. This will improve high frequency response of amplifier.

The Frequency response of CE Amplifier has three regions.

1) LFR.
2) HFR.
3) MFR

TABULATION: V_{IN} :

SL.NO	Input Frequency in (KHZ)	Vout	Gain = 20 log (vout / vin)	Input Frequency (KHZ)	Vout	Gain = 20 log (vout / vin)
1.						
2.						
3.						
4.						
5.						
6.						
7.						
8.						
9.						
10.						
11.						
12.						
13.						
14.						
15.						
16.						
17.						
18.						
19.						
20.						

FREQUENCY RESPONSE CURVE

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as f_L and f_H and are called as the 3dB frequencies (Lower and Upper Cut-Off Frequencies respectively). The difference between higher cut-off and lower cut-off frequency is referred to as bandwidth ($f_H - f_L$).

PROCEDURE: -

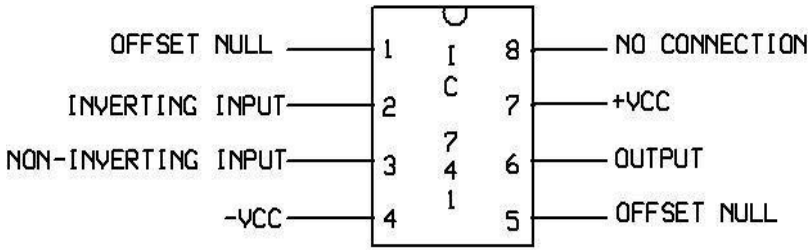
1. The connections are made as per the circuit diagram.
2. The 12v supply is given to the collector terminal.
3. The input voltage is setup as per design value in AFO.
4. By increasing the frequency note down the output voltage and calculate the gain by using the formula.
5. The frequency response was plotted using gain along Y- axis and frequencies along X- axis and from graph calculate the bandwidth by using the formula.

Bandwidth BW = (f2 – f1)

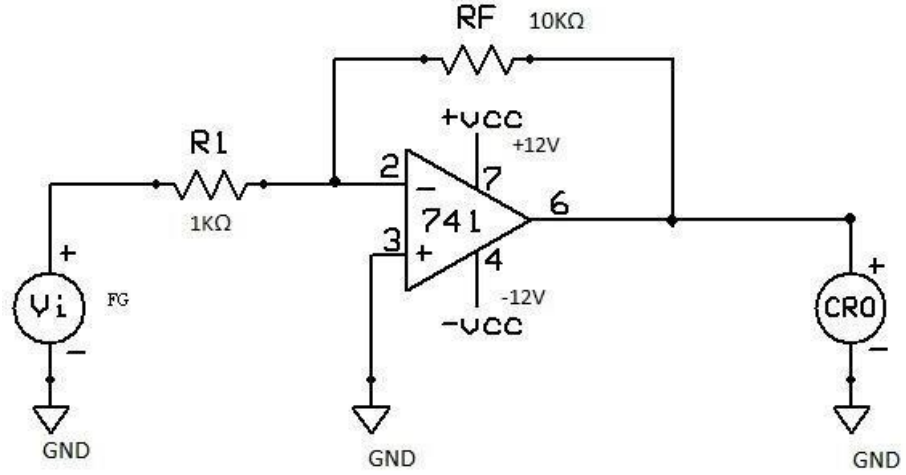
RESULT:

Thus the CE Amplifier was designed and tested and its bandwidth was found to be =_____.

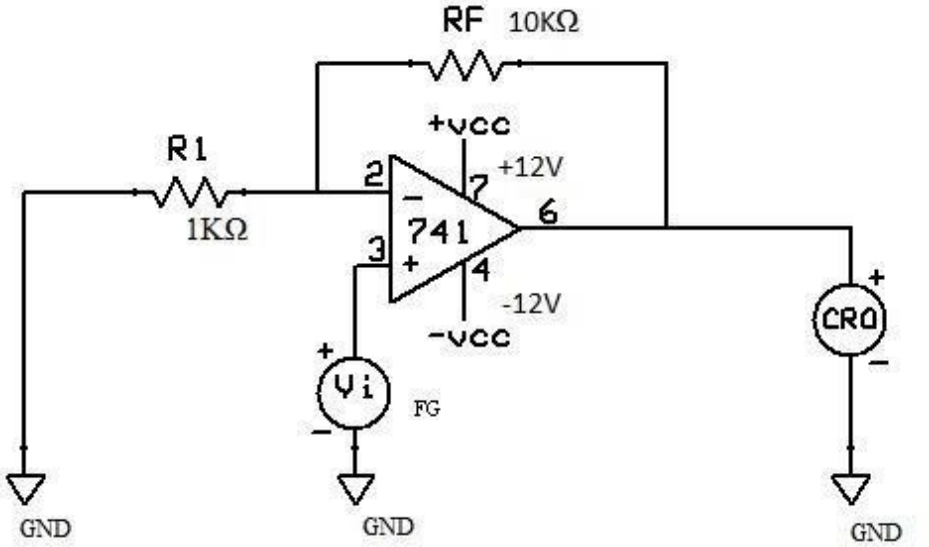
PIN DIAGRAM:



CIRCUIT DIAGRAM: INVERTING AMPLIFIER:



CIRCUIT DIAGRAM: NON INVERTING AMPLIFIER:



EX.NO: **DATE:**

INVERTING AND NON-INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED :

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board	-	1
6.	Resistors		As required
7.	Connecting wires and probes		As required

THEORY:

The input signal Vi is applied to the inverting input terminal through R1 and the non-inverting input terminal of the op-amp is grounded. The output voltage Vo is fed back to the inverting input terminal through the Rf - R1 network, where Rf is the feedback resistor. The output voltage is given as,

$$Vo = - ACL\ Vi$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

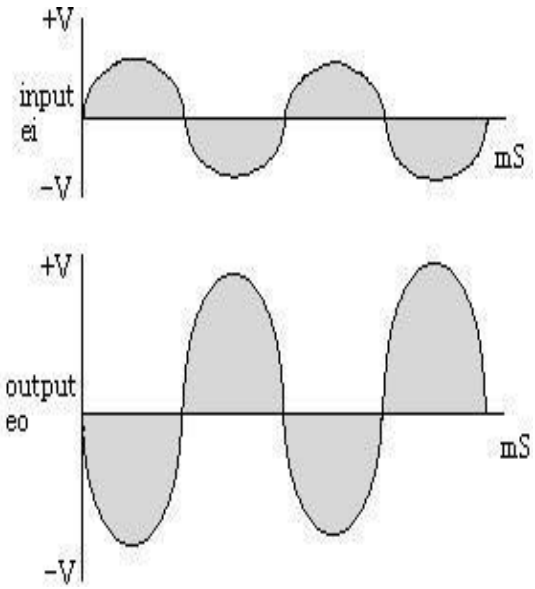
The input signal Vi is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage Vd at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

$$Vo = ACL\ Vi$$

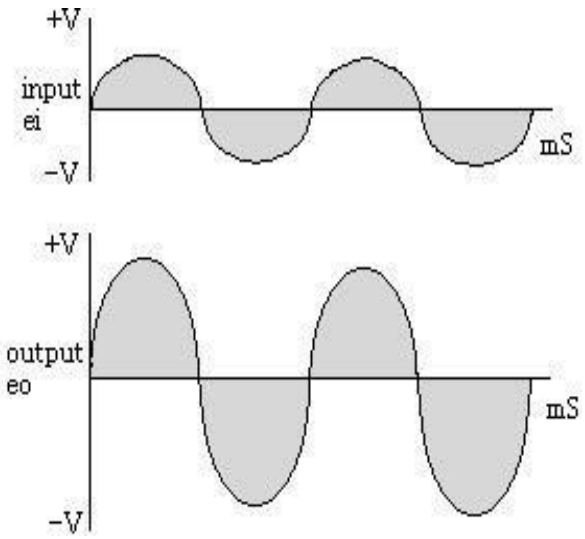
Here the output voltage is in phase with the input signal

Model Graph:

Inverting Amplifier:



Non Inverting Amplifier



TABULATION:

	Inverting Amplifier		Non - Inverting Amplifier	
	Input	**Output**	**Input**	**Output**
Amplitude				
Time				

PROCEDURE:

INVERTING AMPLIFIER:

1. Connections are given as per the circuit diagram.
2. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate inputvoltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms areplotted in a graph sheet

NON-INVERTING AMPLIFIER:

5. Connections are given as per the circuit diagram.
6. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.
7. By adjusting the amplitude and frequency knobs of the function generator, appropriate inputvoltage is applied to the non - inverting input terminal of the Op-Amp.
8. The output voltage is obtained in the CRO and the input and output voltage waveforms areplotted in a graph sheet

DESIGN:

INVERTING AMPLIFIER:

We know that for inverting amplifier

$$ACL = 1+(RF/R)$$

Assume RL (Approximately) 10KΩ and find RF

Hence, $V_O = -ACL * V_i$

NON-INVERTING AMPLIFIER:

We know that for inverting amplifier

$$ACL = RF/R$$

Assume RL (Approximately) 10KΩ and find RF

Hence, $V_O = -ACL * V_i$

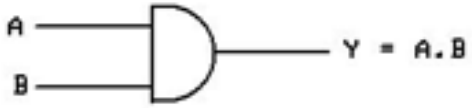
MODEL CALCULATION:

RESULT:

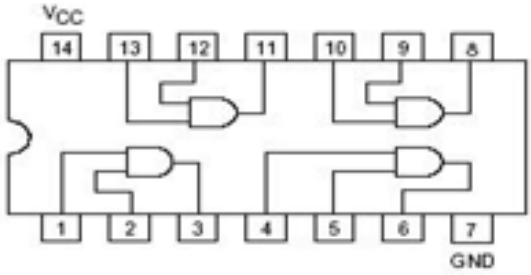
Thus an Inverting Amplifier was designed for the given specifications using Op-Amp IC 741.

AND GATE

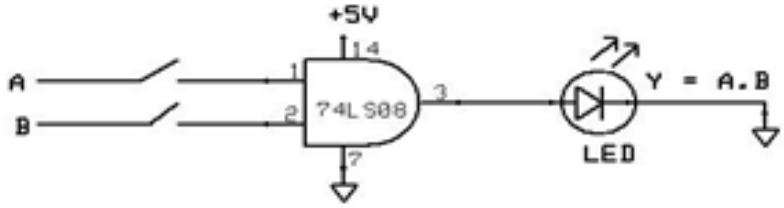
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7408 :



CIRCUIT DIAGRAM:



TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = A . B
1.	0	0	0
2.	0	1	0
3.	1	0	0
4.	1	1	1

EX.NO: **DATE:**

VERIFICATION OF BASIC DIGITAL ICS

AIM:

To verify the truth table of basic digital ICs of AND, OR, NOT, NAND, NOR, EX-OR gates.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit	-	1
2.	AND gate	IC 7408	1
3.	OR gate	IC 7432	1
4.	NOT gate	IC 7404	1
5.	NAND gate	IC 7400	1
6.	NOR gate	IC 7402	1
7.	EX-OR gate	IC 7486	1
8.	Connecting wires	As required	

THEORY:

a. AND gate:

An AND gate is the physical realization of logical multiplication operation. It is an electronic circuit which generates an output signal of '1' only if all the input signals are'1'.

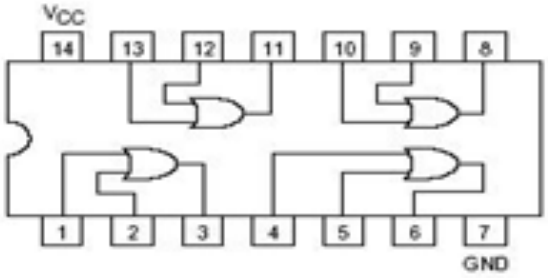
b. OR gate:

An OR gate is the physical realization of the logical addition operation. It is an electronic circuit which generates an output signal of '1' if any of the input signal is '1'.

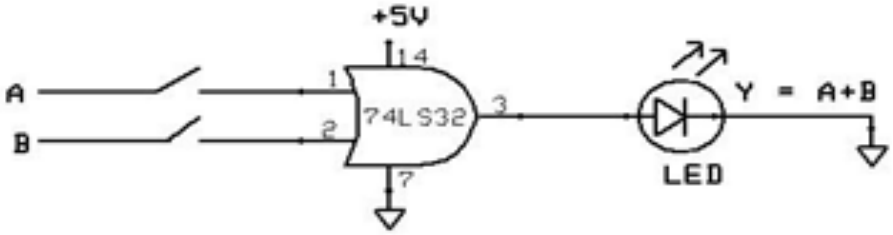
OR GATE

LOGIC DIAGRAM:

PIN DIAGRAM OF IC 7432 :



CIRCUIT DIAGRAM:



TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = A + B
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	1

C. NOT gate:

A NOT gate is the physical realization of the complementation operation. It is an electronic circuit which generates an output signal which is the reverse of the input signal. A NOT gate isalso known as an inverter because it inverts the input.

D. NAND GATE

A NAND gate is a complemented AND gate. The output of the NAND gate will be '0' if all the input signals are '1' and will be '1' if any one of the input signal is '0'.

A NOR gate is a complemented OR gate. The output of the OR gate will be '1' if all the inputsare '0' and will be '0' if any one of the input signal is '1'.

E. Ex-OR GATE

An Ex-OR gate performs the following Boolean function,

$$A \oplus B = (A . B') + (A' . B)$$

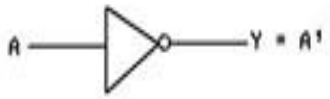
It is similar to OR gate but excludes the combination of both A and B being equal to one. The exclusive OR is a function that give an output signal '0' when the two input signals are equal either '0' or '1'.

PROCEDURE:

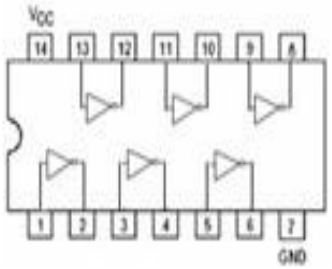
1. Connections are given as per the circuit diagram
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and verify the truth table for all gates.

NOT GATE

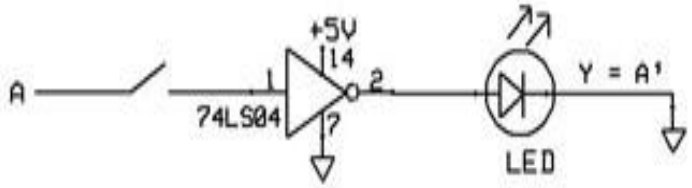
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7404 :



CIRCUIT DIAGRAM:



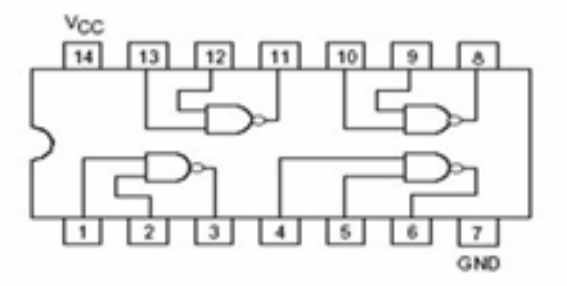
TRUTH TABLE:

S.No.	INPUT	OUTPUT
	A	Y = A'
1.	0	1
2.	1	0

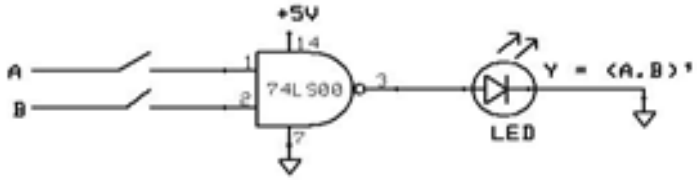
NAND GATE

LOGIC DIAGRAM:

PIN DIAGRAM OF IC 7400 :



CIRCUIT DIARAM:

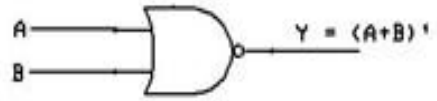


TRUTH TABLE:

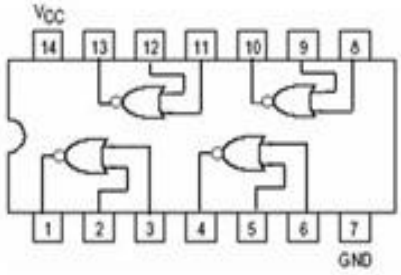
S.No	INPUT		OUTPUT
	A	B	Y = (A. B)'
1.	0	0	1
2.	0	1	1
3.	1	0	1
4.	1	1	0

NOR GATE

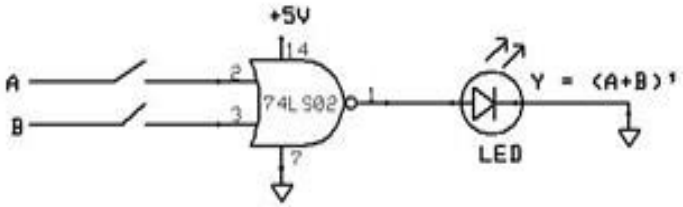
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7402 :



CIRCUIT DIAGRAM:



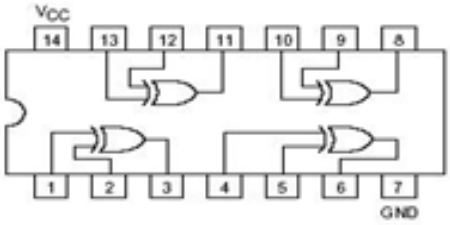
TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = (A + B)'
1.	0	0	1
2.	0	1	0
3.	1	0	0
4.	1	1	0

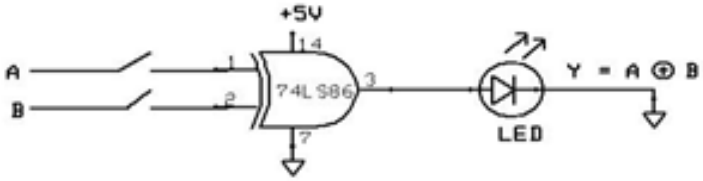
EX-OR GATE

LOGIC DIAGRAM

PIN DIAGRAM OF IC 7486:



CIRCUIT DIAGRAM:



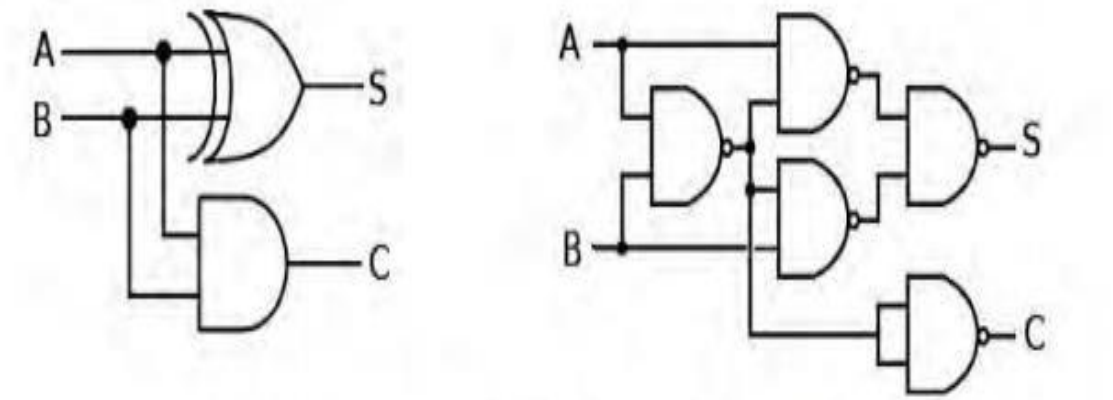
TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = AB⊕
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	0

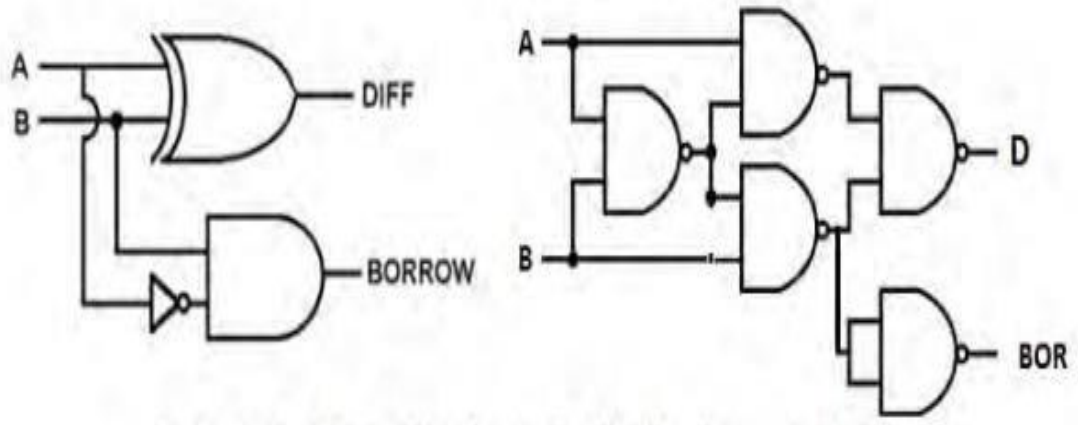
RESULT:

Thus the truth table of all the basic digital ICs was verified.

CIRCUIT DIAGRAM:



Logic circuit of Half adder and Haff adder using NAND gate only



Logic circuit of half subtractor and half subtractor using NAND gates

EX.NO: **DATE:**

DESIGN AND IMPLEMENTATION HALF ADDER AND HALF SUBTRACTOR

AIM

1. To design and set up half adder and half subtractor using
   a. EXOR gates and AND gates
   b. NAND gates

COMPONENTS REQUIRED

IC Trainer kit, IC 7400, IC 7486

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	EXOR gates, AND gates	IC 7474	2
3.	Connecting wires		As required

THEORY

The simplest binary adder is called half adder. Half adder has two input bits and two output bits. One output bit is the sum and the other is the carry. They are represented by'S'and 'C' respectively in logic symbol.

The simplest binary subtractor is called half Subtractor. It has two input bits and two output bits. One output bit is the Difference and the other is borrowed. They are represented by 'D' and 'B' respectively in logic symbol

TABULATION:

Truth table of Half Adder					**Truth table of Half Subtractor**			
Inputs		Output			Inputs		Output	
A	**B**	**S**	**C**		**A**	**B**	**D**	**BOR**
0	0	0	0		0	0	0	0
0	1	1	0		0	1	1	1
1	0	1	0		1	0	1	0
1	1	0	1		1	1	0	0

PROCEDURE:

1. Verify whether all the wires and components are in good condition

2. Set up a half adder circuit and feed all the input combinations

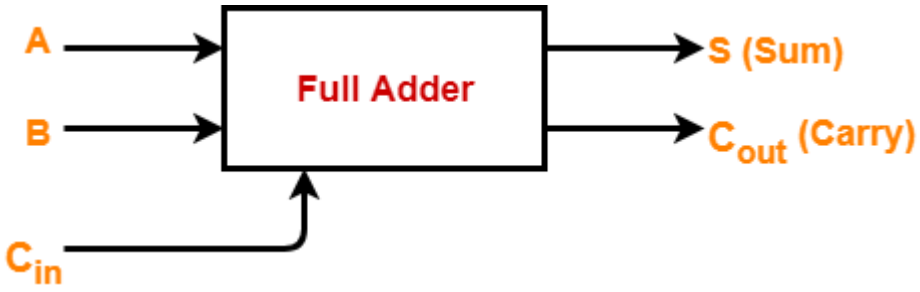
3. Observe the output corresponding to input combinations and enter it in the Truth table

4. Repeat the above steps for half subtractor circuits

RESULT

Half adder and the half subtractor circuits are set up using logic gates and verified the result.

BLOCK DIAGRAM:



TRUTH TABLE

Inputs			Outputs	
A	**B**	**C_{in}**	**S (Sum)**	**C_{out} (Carry)**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

EX.NO: **DATE:**

DESIGN AND IMPLEMENTATION FULL ADDER AND FULL SUBTRACTOR

AIM

1. To design and set up full adder and full subtractor using
   a. EXOR gates and AND gates
   b. NAND gates

COMPONENTS REQUIRED

IC Trainer kit, IC 7432, IC 7486,IC 7408,IC 7400

APPARATUS REQUIRED:

S.No	Components	Quantity
1.	IC 7486,IC 7432,IC 7408, **IC 7400**	2
2.	Digital Trainer Kit	1
3.	Bread Board	1
4.	Connecting Wires	As required

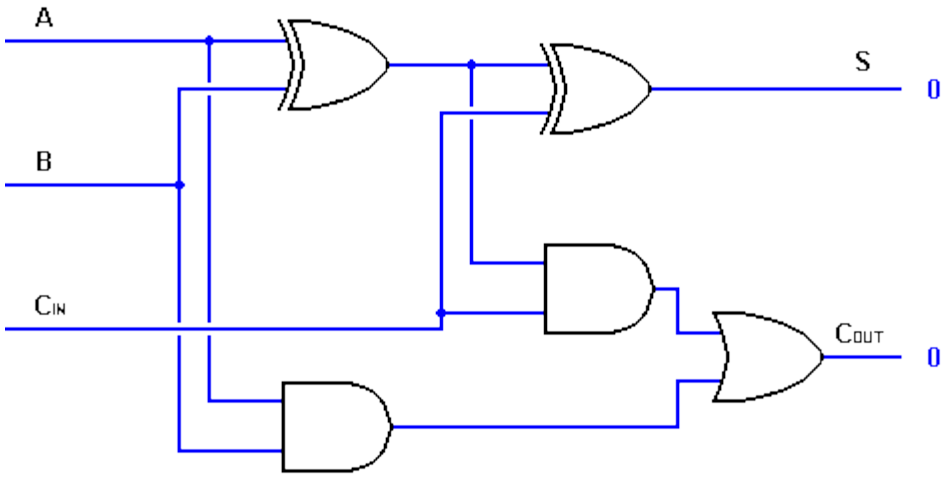
THEORY

❖ The simplest binary adder is called Full adder. Full adder has three input bits and two output bits. One output bit is the sum and the other is the carry. They are represented by‘S’ and ‘C’ respectively in logic symbol.

❖ The simplest binary subtractor is called full Subtractor. It has three input bits and two output bits. One output bit is the Difference and the other is borrow. They are represented by ‘D’ and ‘B’ respectively in logic symbol

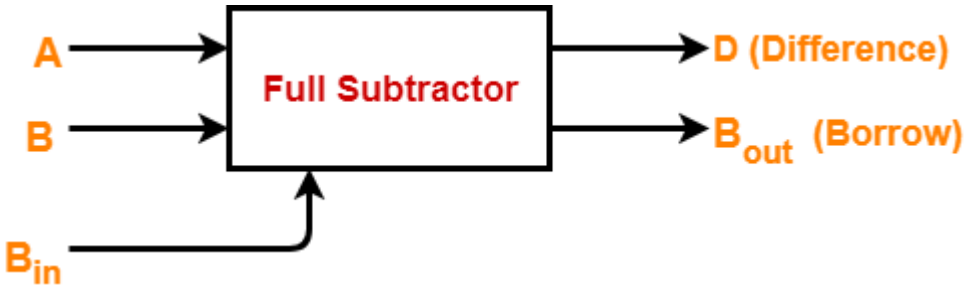
LOGIC DIAGRAM:

FULL ADDER



FULL SUBTRACTOR

BLOCK DIAGRAM:



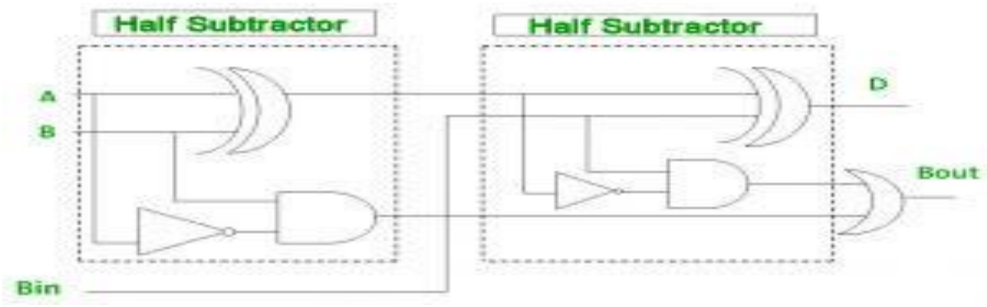
Procedure:

1. Place the required IC on the trainer kit.
2. Make the connections as per the circuit diagram.
3. Connect 7^{th} pin of all IC to ground and 14^{th} pin to +15v.
4. Switch on the supply and verify the circuit as per the circuit truth table.
5. Switch off the power supply and remove the connections.

TRUTH TABLE

Inputs			Outputs	
Minuend (A)	**Subtrahend (B)**	**Borrow (Bin)**	**Difference (D)**	**Borrow (Bout)**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

LOGIC DIAGRAM:



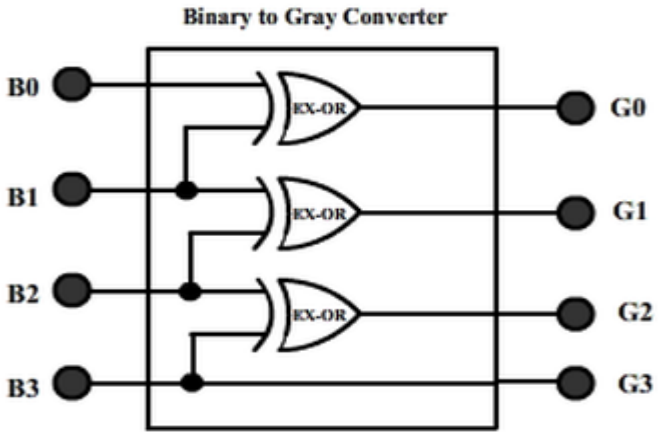
RESULT

Full adder and the Full subtractor circuits are set up using logic gates and verified the result.

TRUTH TABLE: BINARY TO GRAY CONVERSION:

Natural-binary code				Gray code			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

LOGIC DIAGRAM:



EX.NO: **DATE:**

DESIGN AND IMPLEMENTATION CODE CONVERSIONS

AIM:

To design and implement various code conversions.

APPARATUS REQUIRED:

S.No	Components	Quantity
1.	IC 7486	2
2.	Digital Trainer Kit	1
3.	Bread Board	1
4.	Connecting Wires	As required

THEORY:

The availability of a large variety of codes for the same discrete elements of information results in the use of different codes by different digital systems.

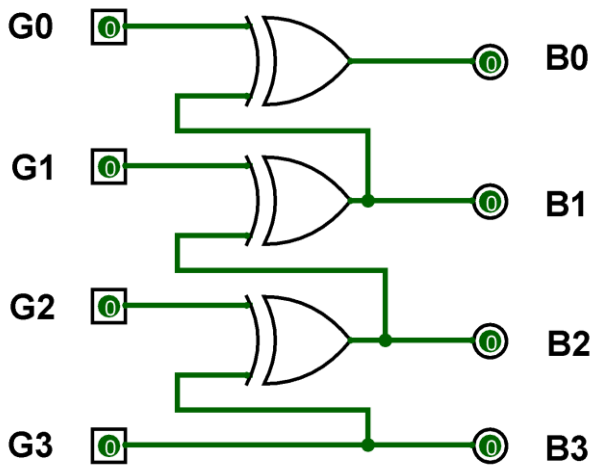
A conversion circuit must be inserted between the two systems if each uses different codes for the same information.

Thus a code converter is a circuit that makes the two systems compatible even though each uses a different binary code. This circuit performs the transformation by means of logic gates.

TRUTH TABLE: GRAY TO BINARY CONVERSION:

Gray code				Natural-binary code			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

LOGIC DIAGRAM:



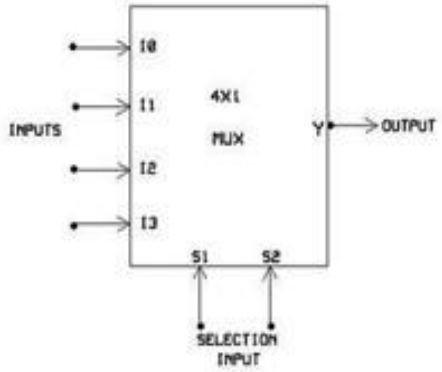
PROCEDURE:

1. Place the required IC on the trainer kit.
2. Make the connections as per the circuit diagram.
3. Connect 7^{th} pin of all IC to ground and 14^{th} pin to +15v.
4. Switch on the supply and verify the circuit as per the circuit truth table.
5. Switch off the power supply and remove the connections.

RESULT:

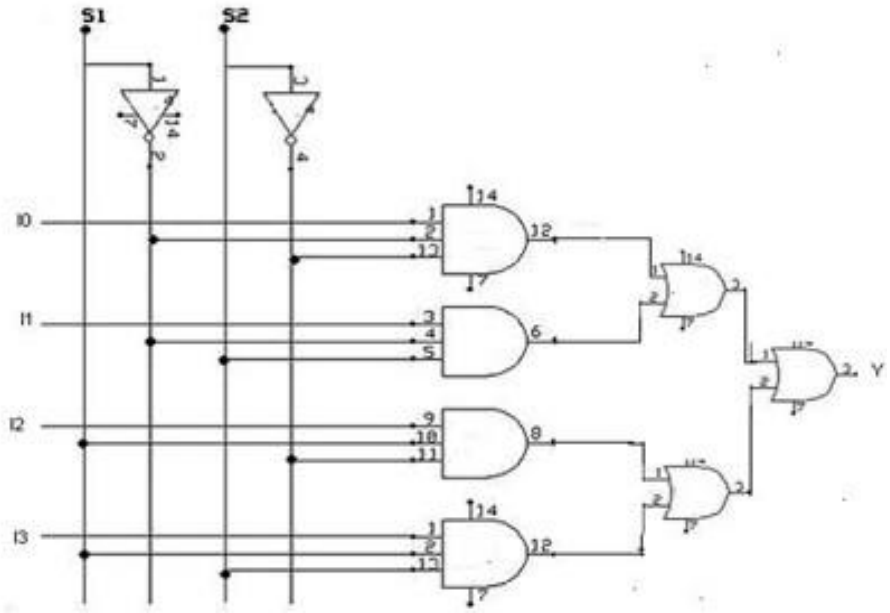
Binary to Gray code Converter and Gray code to Binary code Converter circuits were constructed and their operations were verified.

MULTIFLEXER



TRUTH TABLE:

S.No	Selection Input		Output
	S1	S2	Y
1.	0	0	I0
2.	0	1	I1
3.	1	0	I2
4.	1	1	I3



EX.NO: **DATE:**

DESIGN AND IMPLEMENTATION MULTIPLEXER AND DEMULTIPLEXER

AIM:

To construct the circuit of multiplexer and demultiplexer and to study their working

APPARATUS REQUIRED:

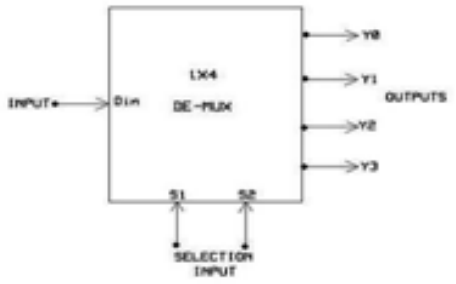
Sl..No	Name of the apparatus	Range	Quantity
1.	Digital IC trainer kit	-	1
2	Connecting wires	-	

THEORY:

A Multiplexer is a combinational logic circuit, which can select any one of the numbersof inputs and route it to a single output. Multiplexers are available with four, eight and sixteeninputs and a single output. It is also called data selector. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides thedigital equivalent of an analog selector switch.

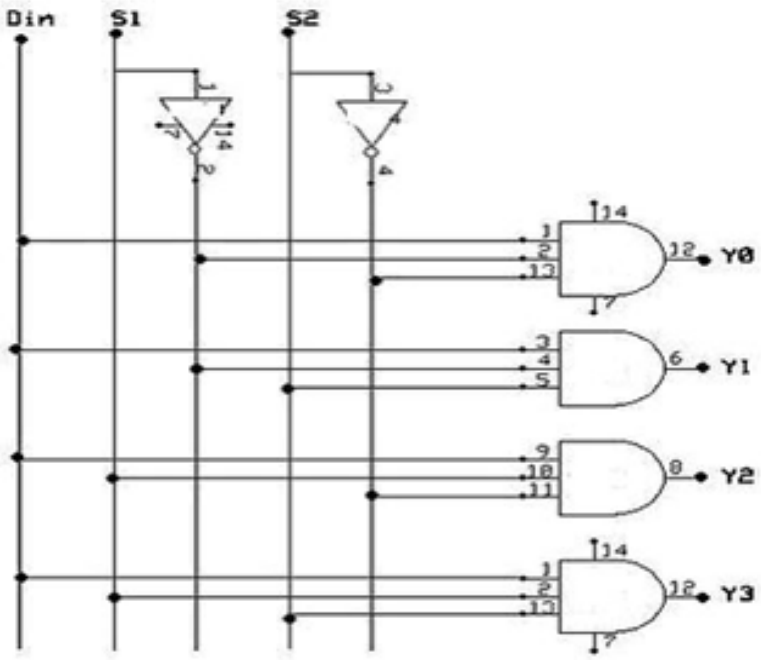
A Demultiplexer has a single input and many outputs. The input to a demultiplexer canbe routed to any of the output channels. For this reason, a demultiplexer is also known as data distributor. The selection of specific output line is controlled by the values of n selection lines.

Demultiplexer:



TRUTH TABLE:

S.No	Input			Output			
	S1	S2	Din	Y0	Y1	Y2	Y3
1.	0	0	0	0	0	0	0
2.	0	0	1	1	0	0	0
3.	0	1	0	0	0	0	0
4.	0	1	1	0	1	0	0
5.	1	0	0	0	0	0	0
6.	1	0	1	0	0	1	0
7.	1	1	0	0	0	0	0
8.	1	1	1	0	0	0	1



PROCEDURE:

A) MULTIPLEXER:

1. Connect the circuit as per the circuit diagram.
2. For various inputs note the corresponding outputs.
3. Verify the truth table of multiplexer.

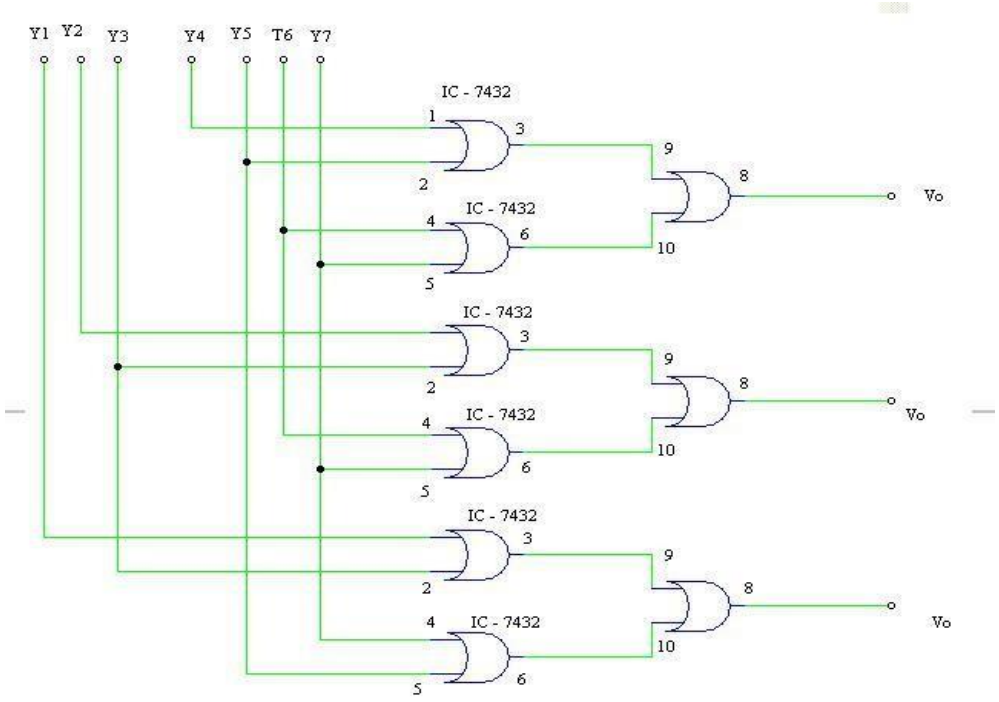
B. DEMULTIPLEXER:

1. Connect the circuit as per the circuit diagram.
2. For various inputs note the corresponding outputs.
3. Verify the truth table of demultiplexer

RESULT:

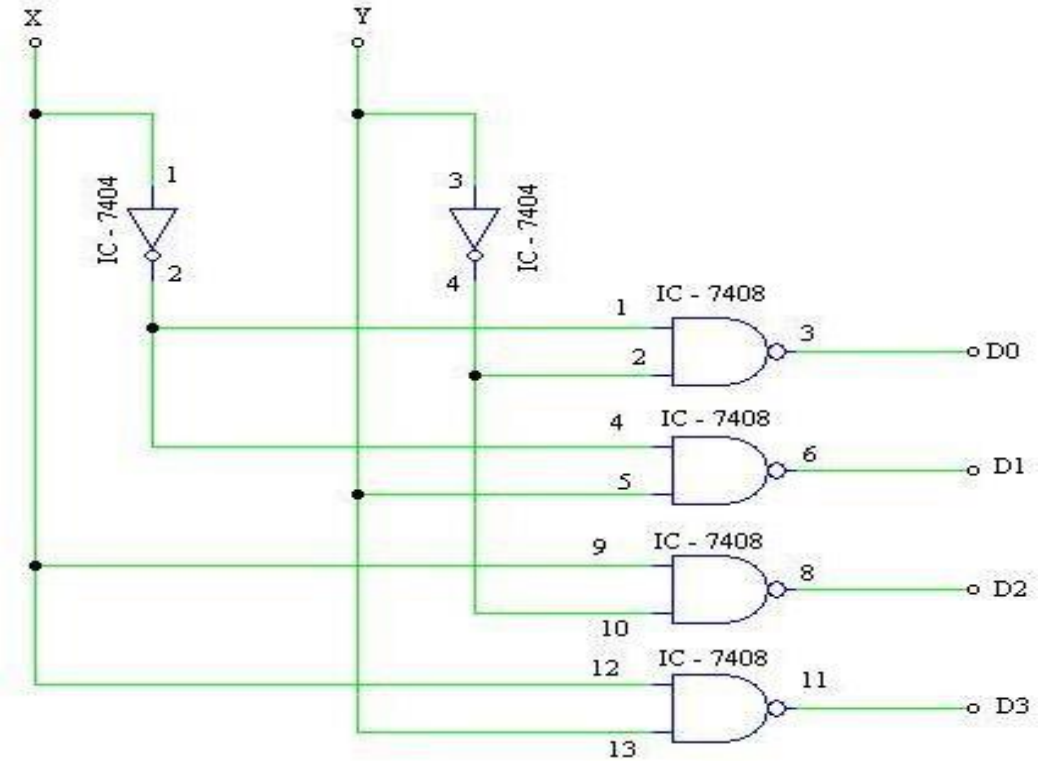
Multiplexer and Demultiplexer circuits were constructed and their operations were verified.

CIRCUIT DIAGRAM: ENCODER



C=Y1 + Y2 +Y3 + Y4

DECODER:



EX.NO: **DATE:**

DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER

AIM:

To design and implement encoder and decoder using logic gates.

APPARATUS REQUIRED:

SL.NO	NAME	RANGE	QUANTITY
1	Nand gate	7408	1
2	OR gate	7432	3
3	NOR gate	7404	1
4	IC trainer kit	-	1
5	Patch chords	-	

THEORY: ENCODER:

An encoder is a digital circuit that performs inverse operation of decoder.An encoder has 2^n input lines and n output lines.An encoder accepts an active level on one of its inputs representing a digit such as a decimal/octal digit and it converts to coded output.Encoder encodes different types of messages into various forms.In digital circuits it encodes a decimalvalue into a binary word.

The encoded binary word has number of bits associated with it.The number of bits depends upon the ddecimal value which is being encoded.For example in case decimal values ranging from 0 to 7 the number of bits required to encode these values is 3.

DECODER:

A decoder is multi input and multi output combinational logic circuit which converts coded input into coded outputs,where the input and output coded are different.

TABULATION: ENCODER:

INPUT							OUTPUT		
Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	A	B	C
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

TABULATION: DECODER:

INPUT			OUTPUT			
E	A_1	A_0	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

PROCEDURE:

ENCODER:

1. Connect the supply from the trainer kit through patch cords;also connect circuit as per circuit diagram.
2. Give the input to A,B &EN through switch.
3. Observe the output Y0 to Y3 on the trainer kit through LED's.

ENCODER:

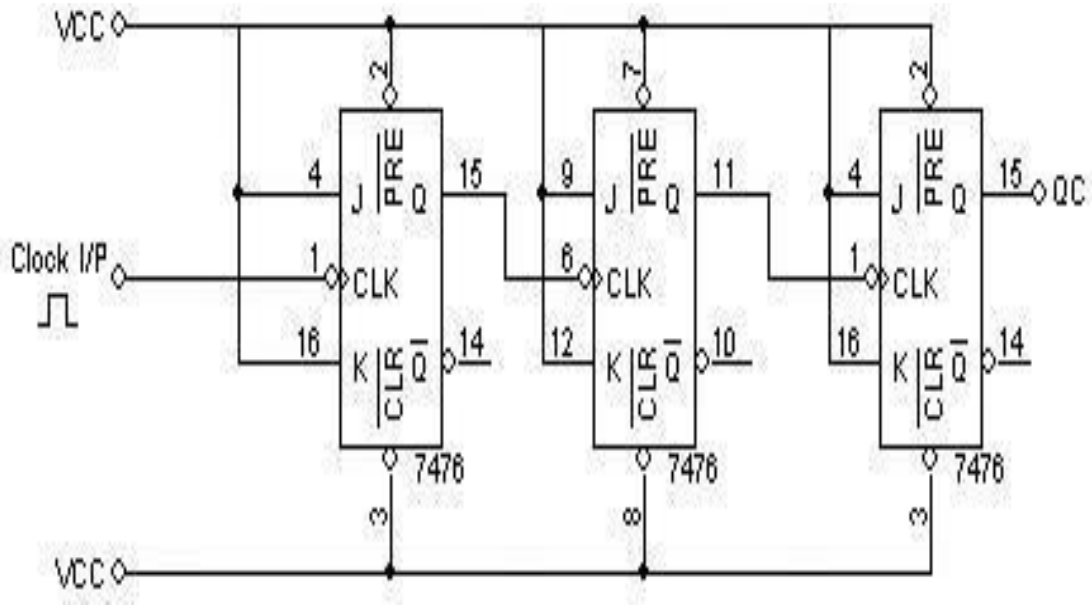
1. Connect the supply from the trainer kit through patch cords; also connect circuit as per circuit diagram.
2. Give the connection to I0,I1,I2 &I3.
3. Observe the output Y0,Y1 on the trainer kit through LED's.

RESULT:

Truth tables of encoder and decoder are verified.

CIRCUIT DIAGRAM:

3-BIT ASYNCHRONOUS UP COUNTER



Clock	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1

EX.NO: **DATE:**

DESIGN AND IMPLIMENTATION OF ASYNCHRONOUS UP & DOWN COUNTER

AIM:

To design and implement the 3 bit up and down counter using IC 7476

APPARATUS REQUIRED: -

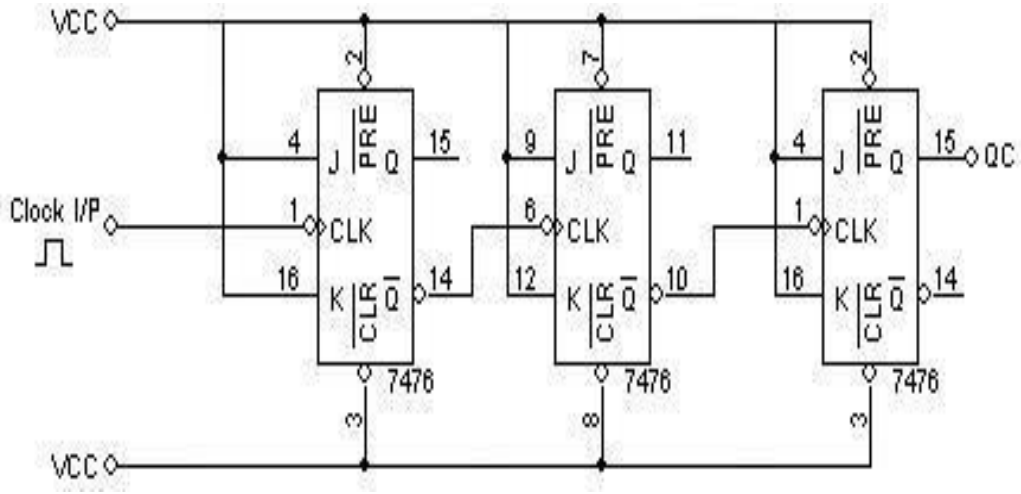
S.No	Name of the Apparatus	Range	Quantity
1.	IC - 7476	-	2
2.	TRAINER kIT		
3.	Bread Board	-	1
4.	Connecting wires and probes		As required

THEORY:

When counter is checked such that each flip flop on the counter is called asynchronous counter. The clock signal is connected to the clock pulse of Ton and Toff condition. The first stage is used to arrive the J and K input at 2nd stage.

CIRCUIT DIAGRAM:

3-BIT ASYNCHRONOUS DOWN COUNTER



Clock	Q_C	Q_B	Q_A
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1
9	1	1	0

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Clock pulses are applied one by one at the clock I/P and the O/P is observed at Q_A, Q_B& Q_C for lC 7476
3. Truth table is verified

RESULT:

Thus the asynchronous up and down counter truth table was verified.