SRI CHANDRASEKHARENDRA SARASWATHI VISWA MAHAVIDYALAYA

(University established under section 3of UGC Act 1956)
(Accredited with 'A' Grade by NAAC)

CURRICULUM FOR FULL TIME

BE - ELECTRONICS AND COMMUNICATION ENGINEERING

HONS./MINOR DEGREE IN EMERGING AREAS(OPTIONAL)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.E. (Hons.) Electronics and Communication Engineering

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B.E /B.TECH-Hons./Minor Degrees in Emerging Areas (Optional)

Emerging Areas	Offered as Hons., for the following Major Disciplines*	Offered as Minor Degrees for the following Major Disciplines**
5G COMMUNICATION SYSTEMS	Electronics and Communication Engineering / Computer Science and Engineering / Information Technology/ Electrical and Electronics Engineering	Electronics and Instrumentation Engineering/ Mechatronics / Mechanical Engineering / Civil Engineering
VLSI DESIGN	Electronics and Communication Engineering / Computer Science and Engineering / Information Technology/ Electrical and Electronics Engineering	Electronics and Instrumentation Engineering/ Mechatronics / Mechanical Engineering / Civil Engineering
IMAGE PROCESSING AND COMPUTER VISION	Electronics and Communication Engineering / Computer Science and Engineering / Information Technology	Electrical and Electronics Engineering /Electronics and Instrumentation Engineering/ Mechatronics/ Mechanical Engineering / Civil Engineering
DRONE TECHNOLOGY	Electronics and Communication Engineering/ Electrical and Electronics Engineering/ Mechatronics/ Mechanical Engineering	Computer Science and Engineering / Information Technology/ Civil Engineering

Note: The "Minor Degree or Hons. will cumulatively require additional 18 to 20 credits in the specified area in addition to the credits essential for obtaining the Under Graduate Degree in Major Discipline.

* Under Graduate Degree Courses in EMERGING AREAS shall be allowed as specialization from the same Department. The minimum additional Credits for such Courses shall be in the range of 18-20 and the same shall be mentioned in the degree, as specialization in that particular area.

** Minor specialization in EMERGING AREAS in Under Graduate Degree Courses may be allowed where a student of another Department shall take the minimum additional Credits in the range of 18-20 and get a degree with minor from another Department.

ELECTRONICS AND COMMUNICATION ENGINEERING WITH HONS./MINOR DEGREES

VLSI DESIGN

CURRICULUM & SYLLABUS

For B.E. (Hons.) Electronics and Communication Engineering with

Specialization inVLSI DESIGN

S.No	Year	Sem	Course Code	Course Name	L	T	P	C	IA	EA	TM
1	II	IV		ANALOG AND DIGITAL IC DESIGN	2	1	0	3	40	60	100
2	III	V		MIXED-SIGNAL AND ARCHITECTURE DESIGN	2	1	0	3	40	60	100
3	III	VI		VLSI SIGNAL PROCESSING	2	1	0	3	40	60	100
4	III	VI		VLSI SIGNAL PROCESSING LABORATORY	0	0	2	2	40	60	100
5	IV	VII		MACHINE LEARNING IN VLSI	2	1	0	3	40	60	100
6	IV	VIII		DEVELOPMENT OF MACHINE LEARNING ALGORITHMS IN VLSI	0	0	2	4	40	60	100
Total Credits					**18**						

Course Code		L	T	P	C	IA	EA	TM
Course Name	**ANALOG AND DIGITAL IC DESIGN**	3	0	0	3	40	60	100
Course Category	PROFESSIONAL SPECIALIZED COURSE	Syllabus Revision					V.1.0	
Pre-requisite	Digital System Design, Microprocessor & Microcontrollers							

Course Objectives:

The course should enable the students

1. To learn combinational and sequential circuits in CMOS design.
2. To learn and design using PLDs.
3. To understand the basics of various analog circuits in VLSI design.
4. To learn FPGA design flow.

Course Outcomes:

On completion of the course, the student will be able to

Course Outcomes	Description	Highest Bloom's Taxonomy
CO1	Design of the combinational and sequential building blocks used indigital CMOS VLSI circuits.	K3
CO2	Analyze and Implement the simple design with PLDs.	K3
CO3	Understand the significance of different analog devices and apply them aptly for different circuits.	K3
CO4	Design all basic building blocks like sources, sinks, mirrors, up to layout level.	K3
CO5	Understand FPGA design flow.	K2

Correlation between Course Outcomes (COs) and Program Outcomes (POs):

COs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	M	L	M	-	-	-	-	-	-	-	-	-	M	M	-
CO2	M	L	M	M	-	-	-	-	-	-	-	-	M	M	-
CO3	M	L	M	M	-	-	-	-	-	-	-	-	M	M	-
CO4	M	L	M	M	-	-	-	-	-	-	-	-	M	S	-
CO5	-	L	M	M	-	-	-	-	-	-	-	-	M	S	-

UNIT-I	**COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS**	**9 Hours**
Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Static Latches and Registers, Dynamic Latches and Registers.		
UNIT-II	**DESIGN EXAMPLES USING PLDs**	**9 Hours**
Design of Universal block, Memory, Floating point, multiplier, Barrel shifter.		
UNIT-III	**INTRODUCTION TO FPGAs**	**9 Hours**
Evolution of programmable devices, FPGA Design flow, Applications of FPGA.		
UNIT-IV	**MOS DEVICES**	**9 Hours**
MOS FET device I/V characteristics, second order effects, Capacitances, body bias effect, Biasing Styles, MOS small signal Model, NMOS verses PMOS devices.		
UNIT-V	**CURRENT MIRROR CIRCUITS**	**9 Hours**
Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks,Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror,Wilson and Widlar current mirrors, voltage and current references.		
	Total Hours	**45 Hours**

Text Book(s)	
1.	Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2.	Design of Analog CMOS Integrated Circuit, Behad Razavi McGraw Hill Education, 2nd Edition, 2017.
Reference Book(s)	
1.	John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.
2.	D.A, Patterson And J.L. Hennessy, Computer Organization and Design: Hardware /Software Interface, 4th Edition, Elsevier, 2011.
3.	Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.

Course Code		L	T	P	C	IA	EA	TM
Course Name	**MIXED-SIGNAL AND ARCHITECTURE DESIGN**	3	0	0	3	40	60	100
Course Category	PROFESSIONAL SPECIALIZED COURSE	**Syllabus Revision**					V.1.0	
Pre-requisite	Analog and Digital IC Design, Microprocessor & Microcontrollers							

Course Objectives:

The course should enable the students

1. To understand mixed signal specifications using op-amp.
2. To analyze the comparators circuits and its requirement in VLSI circuits.
3. To understand the basics of various architecture (RISC/FPGA).
4. To understand the building blocks of FPGA/CPLDs.

Course Outcomes:

On completion of the course, the student will be able to

Course Outcomes	Description	Highest Bloom's Taxonomy
CO1	Design basic cells like OpAmp to meet the mixed signal specifications.	**K4**
CO2	Design comparators to meet the high speed requirements of digital circuitry.	**K4**
CO3	Design of RISC architecture and controller for a specific instruction set.	**K5**
CO4	Understand the building blocks of commercially available FPGA/CPLDs.	**K2**
CO5	Develop models and synthesize targeting for Vertex, Spartan FPGAs.	**K6**

Correlation between Course Outcomes (COs) and Program Outcomes (POs):

COs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO2	PSO3
CO1	M	L	M	-	S	-	-	-	-	-	-	-	M	M	-
CO2	M	L	M	M	S	-	-	-	-	-	-	-	M	M	-
CO3	M	L	M	M	S	-	-	-	-	-	-	-	M	M	-
CO4	M	L	M	M	S	-	-	-	-	-	-	-	M	S	-
CO5	-	L	M	M	S	-	-	-	-	-	-	-	M	S	-

UNIT-I	**OP-AMP CIRCUITS**	**9 Hours**
Basic Building Blocks, OpAmp, Capacitors, Switches, Non-overlapping Clocks, BasicOperation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic- SensitiveIntegrator , Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit.		
UNIT-II	**A/D CONVERTERS**	**9 Hours**
Multi-Bit Successive-Approximation**,** Algorithmic (or Cyclic) A/D Converter, Ratio Independent Algorithmic Converter, Pipelined A/D Converters, One-Bit-Per-Stage Pipelined Converter,1.5 Bit Per Stage Pipelined Converter, Pipelined Converter Circuits.		
UNIT-III	**RISC/CISC**	**9 Hours**
Overview of the features of Instruction set architectures of CISC, RISC processor- Building datapath and Control, multicycle implementation.		
UNIT-IV	**FPGAs/CPLDs**	**9 Hours**
Programming Technologies, Commercially available FPGAs: Xilinx‘s Vertex and Spartan, Actel‘s FPGA, Altera‘s FPGA/CPLD, Building blocks ofFPGAs/CPLDs, Configurable Logic block functionality, Routing structures, Input/outputBlock, Impact of logic block functionality on FPGA performance, Model for measuring delay.		
UNIT-V	**CASE STUDY**	**9 Hours**
Applications using Kintex-7, Virtex-7, Artix-7-Zynq7000 Architecture.		
	Total Hours	**45 Hours**

Text Book(s)	
1.	David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2.	John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.
3.	D.A, Patterson And J.L. Hennessy, Computer Organization and Design: Hardware /Software Interface, 4th Edition, Elsevier, 2011.
Reference Book(s)	
1.	Amano, Hideharu, Principles and Structures of FPGAs, First Edition, Springer, 2018.
2.	Xilinx Inc, Vivado Design Suite User Guide, 2021.
3.	Data sheets of Artix-7, Kintex-7, Virtex-7.

Course Code		L	T	P	C	IA	EA	TM
Course Name	VLSI SIGNAL PROCESSING	3	0	0	3	40	60	100
Course Category	PROFESSIONAL SPECIALIZED COURSE	Syllabus Revision					V.1.0	
Pre-requisite	Digital Signal Processing, Mixed-Signal and architecture Design							

Course Objectives:

The course should enable the students

1. To analyze various VLSI- DSP algorithms in FIR and IIR filters.
2. To analyze algorithm for iteration.
3. To analyze the clocking concepts in DSP Architectures.
4. To implement DSP algorithms in VLSI.

Course Outcomes:

On completion of the course, the student will be able to

Course Outcomes	Description	Highest Bloom's Taxonomy
CO1	Analyze the critical path, iteration bound using LPM and MCM algorithm.	K4
CO2	Analyze Digital filters.	K4
CO3	Apply Retiming, Folding and Unfolding Techniques and Synthesize systolic arrangements.	K4
CO4	Apply Cook Toom and Winograd algorithm and design lookahead and cluster pipelining.	K4
CO5	Ability to modify the existing or new DSP architectures suitable for VLSI.	K6

Correlation between Course Outcomes (COs) and Program Outcomes (POs):

COs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO2	PSO3
CO1	S	M	M	S	S	-	-	-	-	-	-	-	S	S	-
CO2	S	M	M	S	S	-	-	-	-	-	-	-	S	S	-
CO3	S	M	M	S	S	-	-	-	-	-	-	-	S	S	-
CO4	S	M	M	S	S	-	-	-	-	-	-	-	S	S	-
CO5	S	M	M	S	S	-	-	-	-	-	-	-	S	S	-

UNIT-I	**INTRODUCTION TO DSP SYSTEMS**	**9 Hours**
Introduction; representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph.		
UNIT-II	**ITERATION BOUND**	**9 Hours**
Introduction - Loop Bound and Iteration Bound - Algorithms for Computing Iteration Bound: Longest Path Matrix and Minimum Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs.		
UNIT-III	**PIPELINING AND PARALLEL PROCESSING**	**9 Hours**
Pipelining and parallel processing of FIR digital filters, pipeline interleaving in digital filters: signal and multichannel interleaving.		
UNIT-IV	**RETIMING, UNFOLDING AND FOLDING**	**9 Hours**
Retiming techniques; algorithm for unfolding, Folding transformation, systolic architecture design, systolic array design methodology.		
UNIT-V	**FAST CONVOLUTION, FILTERS AND TRANSFORMS**	**9 Hours**
Cook-toom algorithm, modified cook-toom algorithm, Winogard algorithm, iterated convolution Algorithm strength reduction in filters and transforms.		
	Total Hours	**45 Hours**

Text Book(s)	
1.	Keshab k. Parhi, "VLSI Digital Signal Processing Systems: Design and Implementation", Wiley, inter science.
Reference Book(s)	
1.	John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Prentice Hall, Fourth Edition, 2015.
2.	Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing,McGraw-Hill, 2014.

Course Code		L	T	P	C	IA	EA	TM
Course Name	VLSI SIGNAL PROCESSING LABORATORY	0	0	2	2	40	60	100
Course Category	PROFESSIONAL SPECIALIZED COURSE	Syllabus Revision					V.1.0	
Pre-requisite	Digital Signal Processing Lab, CASD Lab							

Course Objectives:

The course should enable the students

1. To provide design concepts on implementation of DSP algorithms in FPGA.
2. To provide insights into design and implementation of image processing.
3. To provide insight on communication protocols used in FPGA domain.

Course Outcomes:

On completion of the course, the student will be able to

Course Outcomes	Description	Highest Bloom's Taxonomy
CO1	Ability to interface external peripherals with a programmable platform.	K5
CO2	Ability to design and implement DSP algorithms into FPGA.	K6
CO3	Ability to analyze and optimize the HDL Code from MATLAB.	K4
CO4	Interpret the ethical principles in engineering practice.	K3
CO5	Express the Engineering activities with effective presentation and report.	K5
CO6	Analyse and develop innovative findings with appropriate technological / research citation.	K6

Correlation between Course Outcomes (COs) and Program Outcomes (POs):

COs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	M	S	S	S	S	-	-	-	-	-	-	-	S	S	-
CO2	S	S	S	S	S	-	L	-	-	-	-	-	S	S	-
CO3	S	S	S	S	S	-	L	-	-	-	-	-	S	S	-
CO4	-	-	-	-	-	-	-	S	S	M	-	M	-	-	S
CO5	-	-	-	-	-	-	-	S	S	M	-	M	-	-	S
CO6	-	-	-	-	-	-	-	S	S	M	-	M	-	-	S

LIST OF EXPERIMENTS	
1.	Implementation of sampling of input signal and display in FPGA.
2.	Implement on DCT, FFT using FPGA.
3.	Synthesize and implement FIR filter and IIR filter Verilog /VHDL.
4.	Experiments on Multirate processing, Bus architectures using FPGA.
5.	Implementation of Application Platforms in FPGA boards.
6.	Image Processing – Image Enhancement, Edge detection.
Tools	
1	MATLAB/HDL

Course Code		L	T	P	C	IA	EA	TM
Course Name	**MACHINE LEARNING IN VLSI**	3	0	0	3	40	60	100
Course Category	PROFESSIONAL SPECIALIZED COURSE	Syllabus Revision					V.1.0	
Pre-requisite	VLSI Design							

Course Objectives:

The course should enable the students

1. To provide a concise introduction to the fundamental concepts of Machine Learning.
2. To explore the different Deep learning techniques including ensemble methods.
3. To gain the knowledge of machine learning to apply in VLSI design.
4. To focus on the backend design challenges, including mask synthesis and physical verification.
5. To study how machine learning can help in physical design.

Course Outcomes:

On completion of the course, the student will be able to

Course Outcomes	Description	Highest Bloom's Taxonomy
CO1	Understand basic applications and issues of Machine Learning.	K2
CO2	Analyze various Machine Learning and Deep Learning techniques and algorithms.	K4
CO3	Apply the knowledge of machine learning in VLSI field.	K4
CO4	Apply the machine learning in physical verification and mask synthesis.	K4
CO5	Predict the machine learning model for physical design such as placement and routing.	K4

Correlation between Course Outcomes (COs) and Program Outcomes (POs):

COs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO2	PSO3
CO1	S	S	M	M	S	-	-	-	-	-	-	-	S	S	-
CO2	L	S	S	S	S	-	-	-	-	-	-	-	S	S	-
CO3	L	S	S	S	S	-	-	-	-	-	-	-	S	S	-
CO4	M	M	M	M	S	-	-	-	-	-	-	-	S	S	-
CO5	M	M	M	M	S	-	-	-	-	-	-	-	S	S	-

UNIT-I	**INTRODUCTION TO MACHINE LEARNING TECHNIQUES**	**9 Hours**
Basics of machine learning Applications of Machine Learning, processes involved in Machine Learning, Supervised Learning, Unsupervised Learning and Reinforcement Learning, Evaluation Measures: confusion matrix, precision, recall, F-Score, ROC-Curve, Cross-Validation.		
UNIT-II	**DEEP LEARNING: CONVOLUTIONAL NEURAL NETWORKS**	**9 Hours**
Feed forward networks, Activation functions, back propagation in CNN, optimizers, batch normalization, convolution layers, pooling layers, fully connected layers, dropout, Examples of CNNs.		
UNIT-III	**MACHINE LEARNING IN VLSI DESIGN**	**9 Hours**
A Taxonomy for Machine Learning in VLSI Design Energy-Efficient Design of Advanced Machine Learning Hardware.		
UNIT-IV	**MACHINE LEARNING APPLICATIONS IN IC VERIFICATION**	**9 Hours**
ML in Physical Verification, Layout Feature Extraction and Hotspot Detection, ML in Mask Synthesis, Mask Synthesis Flow, Mask Synthesis and Verification, Machine Learning for Clock Optimization, Decision tree induction algorithm, Importance of Lithographic Patterning Process. Machine Learning for Lithography.		
UNIT-V	**MACHINE LEARNING APPLICATIONS IN IC PHYSICAL DESIGN**	**9 Hours**
Machine Learning for Physical Design: Modern VLSI Layouts, Placement and Routing Example, Correlation between Placement and Routing, Machine Learning for Placement, Routing, Mask Synthesis and Verification, VLSI Placement and Algorithm, Challenges for VLSI Design, Routability-Driven Placement, Prediction of Routing Congestion, Challenges of Routing Congestion, Application Specific ML.		
	Total Hours	**45 Hours**

Text Book(s)	
1.	Ethem Alpaydin, Introduction to Machine Learning, PHI.
2.	Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds. Machine Learning in VLSI Computer-Aided Design. Springer, 2019.
Reference Book(s)	
1.	Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verlag.

Course Code		L	T	P	C	IA	EA	TM
Course Name	**DEVELOPMENT OF MACHINE LEARNING ALGORITHMS IN VLSI**	0	0	2	4	40	60	100
Course Category	PROFESSIONAL SPECIALIZED COURSE	Syllabus Revision					V.1.0	
Pre-requisite								

Course Objectives:

The course should enable the students

1. To carry out research / investigation and development work and to solve practical problems in the field of VLSI.
2. To Write and present a substantial technical report / document in the field of VLSI.
3. To Demonstrate the Research findings the VLSI area.

Course Outcomes:

On completion of the course, the student will be able to

Course Outcomes	Description	Highest Bloom's Taxonomy
CO1	Synthesize knowledge and skills previously gained and apply to an in-depth study and execution of new technical problems in the area of VLSI.	K3
CO2	Define specification, adopt new VLSI methodologies and analyze to produce a suitable research design and justify the design.	K5
CO3	Demonstrate the research findings through hardware and software tools.	K5
CO4	Present the findings of their technical solution in a written report.	K6
CO5	Publish the work in reputed journals and International Conferences.	K6

Correlation between Course Outcomes (COs) and Program Outcomes (POs):

COs	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	S	S	S	S	S	-	-	-	-	-	-	M	S	S	-
CO2	S	S	S	S	S	S	S	-	-	-	-	S	S	S	-
CO3	-	-	S	S	S	S	S	-	-	-	S	M	S	S	-
CO4	-	-	-	-	-	-	-	S	S	M	-	S	-	-	S
CO5	-	-	-	-	-	-	-	S	S	M	-	M	-	-	S

PRACTICAL SYLLABUS:	
The project topic should be selected to ensure the satisfaction need to establish a direct link between education, national development and productivity and reduce the gap between the world of work and the world of study. The project should have the following	
1.	Relevance to social needs of society.
2.	Relevance to value addition to existing facilities in the institute.
3.	Relevance to industry need.
4.	Problems of national importance.
5.	Research and development in various domain.
The student should complete the following for Mini Project	
1	Literature survey and Problem Definition.
2	Motivation for study and Objectives.
3	Preliminary design approaches.
4	Development and Verification.
5	Report and presentation.
6	Presenting the work in Reputed journals / International Conferences.
Examples	
1	Design and Development of a Bayes Classifier for Two-Class and Multi-Class Classification.
2	Design and Development of a Deep Learning Classifier Model.
3	Design and Development of Clustering Algorithms.
4	Develop the algorithms using Raspberry Pi.